SIM6800M Series High Voltage 3-Phase Motor Driver ICs

Introduction

The SIM6800M series is an inverter power module which includes power MOSFETs or IGBTs, pre-driver IC, and bootstrap diodes with limit resistors in a single package. The device provides an ideal solution especially for small size inverter motors such as fans and pumps. These ICs take 230 VAC input voltage, and up to 5 A (continuous) output current. Figure 1 shows the functional block diagram of the device.

High voltage power supply is applied between VBB and LSx. 15 V is applied between VCC1 and COM1, and VCC2 and COM2. Six signals, HIN1 through HIN3 and LIN1 through LIN3, control the on-off switching of the six internal power MOSFETs or IGBTs. These input signals are active high (xIN = High → MOSFET on). Boot capacitors should be connected between VB1A or VB1B and U, VB2 and V, and VB3 and W1, for high-side power supply.

The device includes: OCP (overcurrent protection, activated for example at a short on the inverter bridge), TSD (thermal shutdown, activated for example at abnormal temperatures, or overloads), and UVLO (protection circuit for sudden drops of the controlling power supply voltage). Operation of these protection features can be monitored on the fault signal output pin, $\overline{FO}$.

There is a current limiter function for the MOSFET or IGBT control signal. When the current through a shunt resistor exceeds the threshold, the OCL pin goes high (active high). By connecting this signal to the SD pin, current limiter operation (high-side of MOSFETs or IGBTs turned off for 1 carrier PWM cycle) can be performed.

Table 1. SIM6800M Series Lineups

Part Number	Power Device Rating					Boot Resistance (Ω)	Input Voltage (VAC)	Note
	Type	Breakdown (V)	Output (A)	$R_{DS(ON)}$ (Ω) (Typ)	$R_{DS(ON)}$ (Ω) (Max)			
SIM6812M	MOSFET	500	2.5	2.0	2.4	60	200	–
SIM6813M	MOSFET	500	3.0	1.4	1.7	60	200	–
SIM6822M	IGBT	600	5.0	$V_{CE(sat)}$ (V) (Typ) 1.75	$V_{CE(sat)}$ (V) (Max) 2.2	60	200	Low switching loss
SIM6827M								Low noise

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Features

• Package: 40-pin DIP

The SIM6800M series is packaged in a DIP package with 29 pins, which enables down-sizing and simple PCB layout. Pin pitch is 1.778 mm, with a 3.556 mm pitch separating adjacent high and low voltage pins. Pin width is 0.52 mm. Body thickness is 4.0 mm.

• Three built-in high voltage bootstrap fast recovery diodes (FRD) diodes, each with current limiting resistor and capable of withstanding high voltages: 600 V at 0.5 A

• OCL (Overcurrent Limiter) function (with shutdown (SD) input pin)

When the current exceeds the maximum current level value, V_{lim}, to limit the current, the high-side MOSFETs or IGBTs are switched off for one PWM cycle at the carrier frequency.

• OCP (Overcurrent Protection)

OCP is a function that shuts down the low-side MOSFET or IGBT gate signal at overcurrent conditions, such as output short-circuit and inverter bridge short-circuit, and to output an alarm signal. The output time of the alarm signal is set by an external resistor and capacitor.

• Gate shutdown function on both high- and low-side at abnormal operation

Externally connecting the SD pin and the inverted $\overline{FO}$ pin signal enables the device to shut down all high-side and low-side MOSFETs at abnormal conditions (when the $\overline{FO}$ signal goes low), such as overheating, overcurrent, or controlling power supply voltage drop.

• Built-in TSD (thermal shutdown) function, embodied in the low-side driver IC (MIC)

When the MIC chip temperature exceeds the set value, the gate input is shut down, and the device outputs an alarm signal. Temperature is monitored by the low-side MIC.

• Built-in protection circuit for controlling power supply voltage drop (UVLO)

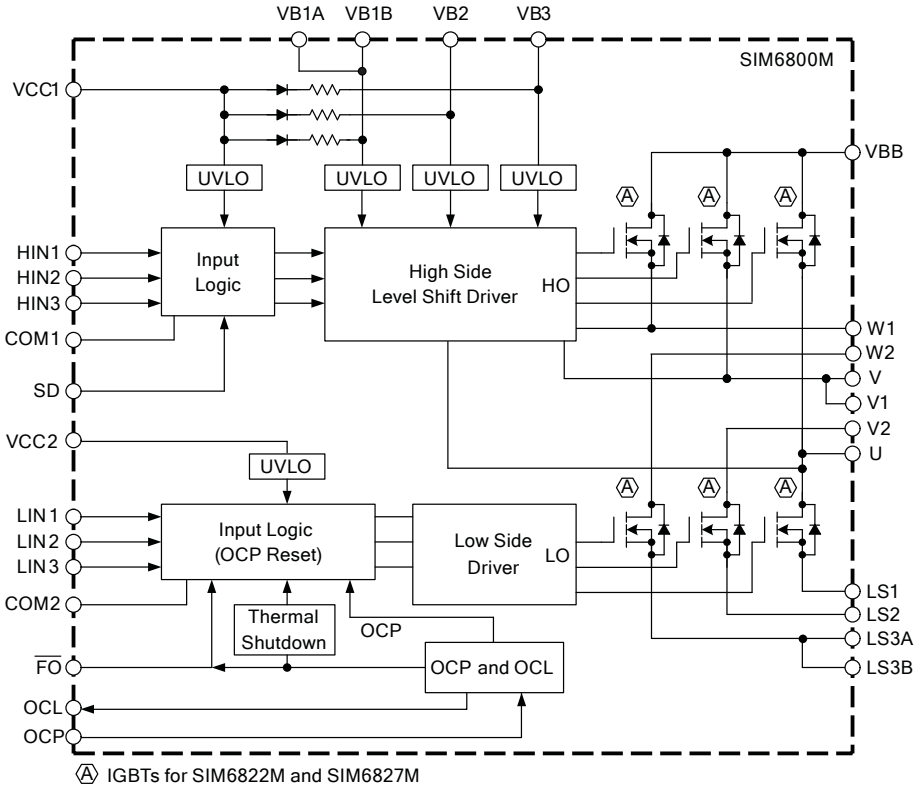


Figure 1. Functional Block Diagram

The device monitors each controlling supply voltage: VCC1, VCC2, and VBx. If any of these voltages falls below the undervoltage threshold, the gate is shut down. If the VCC2 voltage falls below the undervoltage threshold, the $\overline{FO}$ signal is asserted.

• Alarm signal output (indicating shut down) while protection circuit is in operation

Operates on the low, through the $\overline{FO}$ pin, an open collector output. When TSD, OCP, or UVLO protection for controlling power supply voltage VCC2 drop are activated, the internal transistor turns on and drives the $\overline{FO}$ pin low.

• RoHS compliance

RoHS compliant (Pb free) for pin solder and internal solder.

• Structure

The SIM6800M series has six MOSFET or IGBT chips , two drive ICs, and three bootstrap fast recovery diodes mounted on a copper leadframe. Gold wires connect from chip to chip, and from chip to leadframe. The case is molded epoxy resin. Part number and lot number are printed on the surface of the case. Figure 2 shows the package exterior.

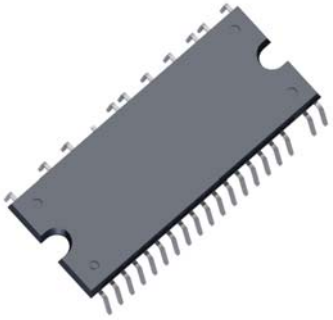


Figure 2. SIM6800M Package Structure: external view

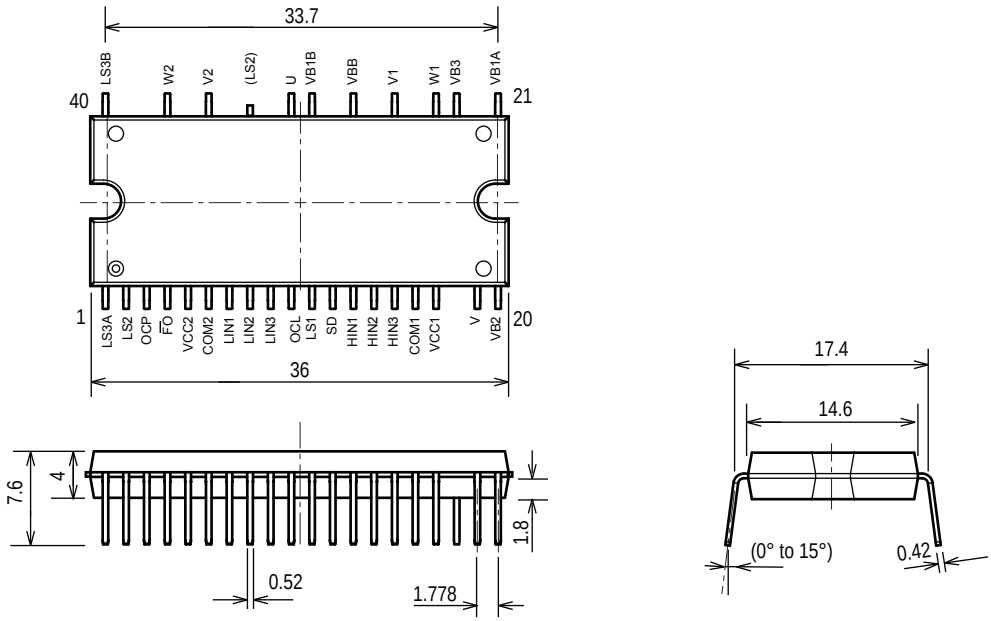
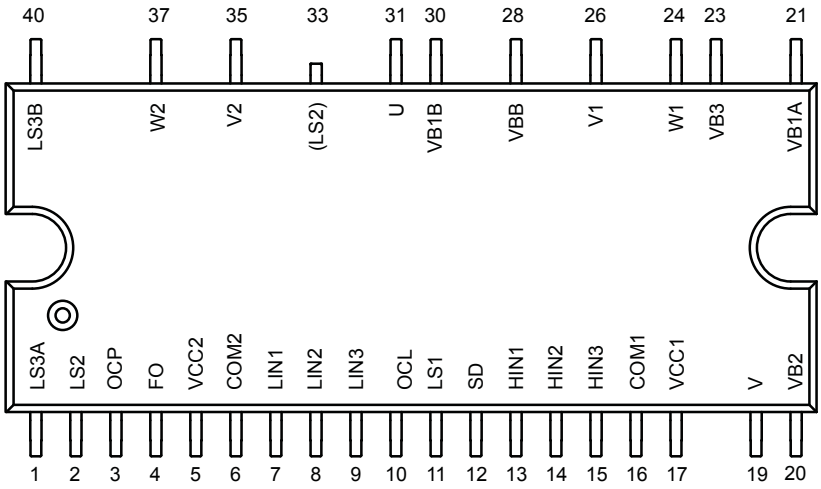


Figure 3. SIM6800M Package Outline Drawing

Pin Functions

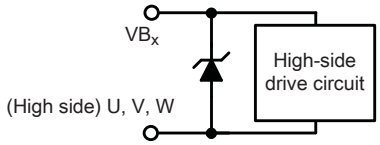
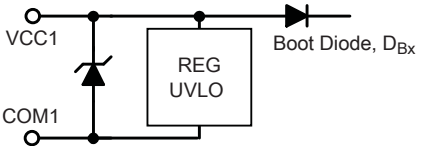
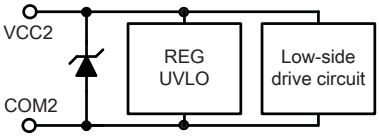
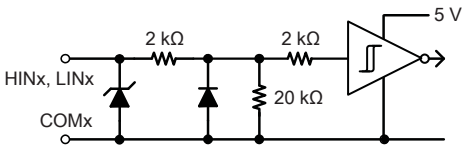
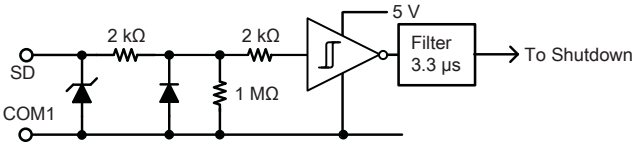
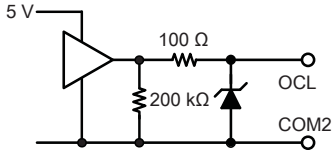
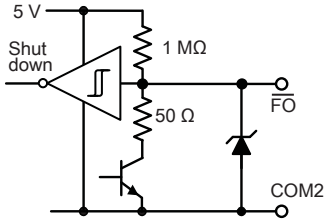
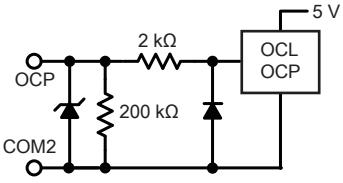


To keep sufficient distance between high and low voltage pins, or between high-voltage pins with different electric potentials, one pin each is removed between: pin 17 (VCC1) and pin 19 (V), pin 21 (VB1A) and pin 22 (VB3), pin 24 (W1) and pin 26 (V1), pin 26 (V1) and pin 28 (VBB), pin 28 (VBB) and pin 30 (VB1B), pin 31 (U) and pin 33 (LS2), pin 33 (LS2) and pin 35 (V2), and pin 35 (V2) and pin 37 (W2), and two pins between pin 37 (W2) and pin 40 (LS3B).

Table 2. Pin List Table

Number	Name	Function	Number	Name	Function
1	LS3A	Source pin, W phase (MOSFET) Emitter pin, W phase (IGBT), connected to LS3B internally	17	VCC1	High-side logic supply voltage
2	LS2	Source pin, V phase (MOSFET) Emitter pin, V phase (IGBT) (pin 33 has same function, but is trimmed)	18, 22, 25, 27, 29, 32, 34, 36, 38, 39	–	Pin deleted
3	OCP	Input for overcurrent protection			
4	$\overline{\text{FO}}$	Fault signal output; active low	19	V	High-side bootstrap negative pin (V phase)
5	VCC2	Low-side logic supply voltage	20	VB2	High-side bootstrap positive pin (V phase)
6	COM2	Low-side logic GND pin	21	VB1A	High-side bootstrap positive pin (U phase), connected to VB1B internally
7	LIN1	Low-side input pin (U phase)	23	VB3	High-side bootstrap positive pin (W phase)
8	LIN2	Low-side input pin (V phase)	24	W1	Output of W phase (connect to W2 externally)
9	LIN3	Low-side input pin (W phase)	26	V1	Output of V phase (connect to V2 externally)
10	OCL	Overcurrent limiting (OCL) signal output	28	VBB	Main supply voltage
11	LS1	Source pin, U phase (MOSFET) Emitter pin, U phase (IGBT)	30	VB1B	High-side bootstrap positive pin (U phase), connected to VB1A internally
12	SD	High-side shutdown input	31	U	Output of U phase
13	HIN1	High-side input pin (U phase)	33	(LS2)	Source pin, V phase (MOSFET) Emitter pin, V phase (IGBT) (pin trimmed, see pin 2 for same function)
14	HIN2	High-side input pin (V phase)	35	V2	Output of V phase (connect to V1 externally)
15	HIN3	High-side input pin (W phase)	37	W2	Output of W phase (connect to W1 externally)
16	COM1	High-side logic GND pin	40	LS3B	Source pin, W phase (MOSFET) Emitter pin, W phase (IGBT), connected to LS3A internally

Table 3. Equivalent Circuits for Input and Output Pins

Pin Number	Pins	Input or Output	Equivalent Circuit
21(30) 20 23	VB1A(VB1B) VB2 VB3	Regulator	
17	VCC1	Regulator	
5	VCC2	Regulator	
13 14 15 7 8 9	HIN1 HIN2 HIN3 LIN1 LIN2 LIN3	Input	
12	SD	Input	
10	OCL	Output	
4	$\overline{FO}$	Input, Output	
3	OCP	Input	

Descriptions of input and output pins

The following are explanations for the input and output pins (please refer to figure 18):

• VBB pin

This is the main supply voltage pin.

Note: In order to reduce surge voltages, it is recommended to use a snubber capacitor, C_S in figure 18, of 0.01 to 0.1 µF between VBB and COM. In order to achieve better effectiveness of the snubber capacitor, please make the capacitor PCB trace as short as practicable, and place it between the IC and an additional electrolytic capacitor.

VBB is a high voltage pin. Please provide sufficient separation from other traces or consider using overcoating material.

In addition, the main current flows through VBB. Please make these traces as wide as possible.

• U, V, V1, V2, W1, W2 pins

These pins are connected to the motor. Because V1 and V2, and W1 and W2, are not connected to each other internally in the IC, please connect those pins on the PCB. Because these output pins have high voltage, please provide sufficient separation from other traces or consider using overcoating material.

Note: Because the V pin is internally connected the V1 pin, there is no requirement to connect these two pins to each other externally. The V pin is used to connect the bootstrap capacitor. Please do not connect this pin to the motor.

Because the main current flows through the U, V1, V2, W1, and W2 pins, please make the traces wide for these pins.

• LS1, LS2, LS3A (LS3B) pins

These are GND pins and shunt resistor sensing pin of the main power supply. Please connect the current detection shunt resistor(s) between these pins and the COM pins.

Because LS3A and LS3B are connected internally, it is not necessary to connect them externally. You can either use LS3A or LS3.

By inputting a current detection signal into the OCP pin, the current limiter circuit function and overcurrent protection are enabled. The LSx pins and the shunt resistor should be connected with the shortest possible trace length. If the trace is long, it will be a factor for malfunctions due to parasitic inductance. Please make the connection between the LSx and COM pins low impedance (the LSx potential is less than –3 V when a motor drive is operating).

• VB1A (VB1B), VB2, VB3 pins

These are pins to connect the bootstrap capacitors for the high-side controlling supply voltage. Please connect individual capacitors, C_{BOOTx}, between VB1A(VB1B) and U, VB2 and V, and VB3 and W1. VB1A is internally connected to VB1B. Connect to either VB1A or VB1B.

In order to avoid effects of external noise, please place these capacitors very near to the IC. In addition, please use ceramic capacitors which have good high frequency response.

The bootstrap capacitors are charged from the VB pins, which are supplied through the VCC1 pin, the bootstrap diodes, D_B, inside the IC, and the in-rush current limiter boot resistors, R_B. The time constant for charging is $R_B \times C_B$.

• VCC1, VCC2 pins

These are the control power supply voltage pins. Please connect both VCC1 and VCC2 to 15 V. To avoid malfunction or damage by power supply ripple or external surges, please put ceramic capacitors, C_{BYP}, of 0.01 to 0.1 µF near the pins. In addition, if surge voltage could exceed 20 V, it is recommended to use a Zener diode, D_Z (V_Z = 18 to 20 V) .

• HIN1, HIN2, HIN3, LIN1, LIN2, and LIN3 pins

These are the input pins for MOSFET or IGBT control. Threshold voltage is set for the use of both 3.3 V and 5 V inputs. In case external noise becomes significant or wire connections are long, please consider using an RC filter, as shown in figure 4 (R_A = 50 to 300 Ω, C = 100 to 1,000 pF), or a pull-down resistor (R_{PD} ≈ 4.7 to 10 kΩ).

• SD pin

This input pin is used to shut down the high-side output MOSFETs. The pin is active high, and when a high signal (3.3 or 5 V) is applied, those MOSFET gates are shut down.

By connecting OCL to the SD pin externally, current limiter operation is enabled (figure 6 shows the timing diagram for the current limiter function). There is an internal filter of 3.3 µs (typ) on the SD pin. Pulses input from the OCL pin that are narrower than that are considered noise, and the gates are not shut down. If a pulse is wider than 3.3 µs, the gates are shut down. When the gates are shut down, the current flowing through the shunt resistor becomes 0 A, and the OCL signal goes low (0 V), However, each high-side MOSFET remains off until the corresponding HIN signal transitions from low to high, until a positive (rising) signal edge comes (referred to as *edge operation*).

By connecting the SD pin and the inverted $\overline{FO}$ pin signal, all high-side and low-side MOSFETs can be shut down when an abnormal circumstance occurs, such as overheating, overcurrent, or undervoltage on the control supply voltage.

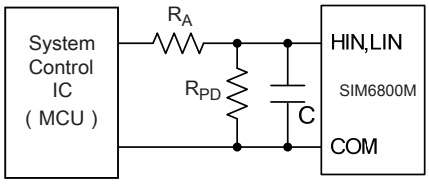


Figure 4. External Noise Reduction Circuit; for HIN and LIN input pins

• OCL, OCP pins

As shown in figure 5, the OCP pin can be used to control the OCL pin. The LSx pins are externally connected to the OCP pin; if the connection is not made, the OCL and OCP functions are not enabled. If the voltage at the LSx pins is kept higher than 0.65 V (typ) for 2 µs (typ), the output voltage at the OCL pin goes high (5 V). When OCL is connected to the SD pin, it operates as a current limiter (see figure 6 for current limiter timing).

• $\overline{FO}$ pin

An internal transistor on the $\overline{FO}$ output pin is turned on by the protection circuits due to overcurrent, overtemperature, or for undervoltage on the control supply voltage, V_{CC2}. At the same time, the low-side MOSFETs or IGBTs are shut down. After the fault condition is released, the LO operates according to LIN (logic level operation).

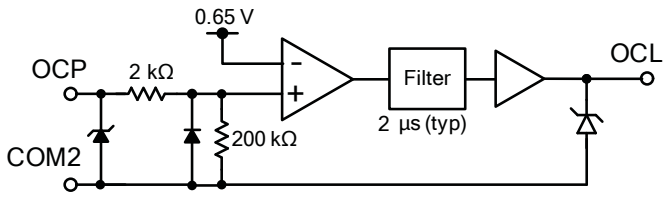


Figure 5. Equivalent Circuit from OCP to OCL

Please connect a pull-up resistor, R_{FO} = 3.3 to 10 kΩ, and a capacitor for noise malfunction prevention, C_{FO} = 0.001 to 0.01 µF, to the $\overline{FO}$ pin.

Protection Functions

The following are descriptions and timing charts of the operation of protection functions for the SIM6800M series.

Protection circuit for controlling power supply voltage drop (undervoltage lockout, UVLO)

If gate drive voltage of the output MOSFETs becomes insufficient, there is greater MOSFET power dissipation, and in the worst case, the IC may be damaged. In order to avoid this, a protection circuit for controlling power supply voltage drop is incorporated.

The control IC (MIC) monitors the high-side voltage: between VCC1 and COM1, VB1A(VB1B) and U, VB2 and V, and VB3 and W1 (the MIC also monitors the low-side voltage, between VCC2 and COM2). As shown in figure 7, after V_B exceeds the V_{UVHH} rated value, 10.5 V (typ), at the next positive (rising) edge on HIN (edge operation), an output-on pulse appears at HO (the gates of the high-side output MOSFETs). When V_B goes below

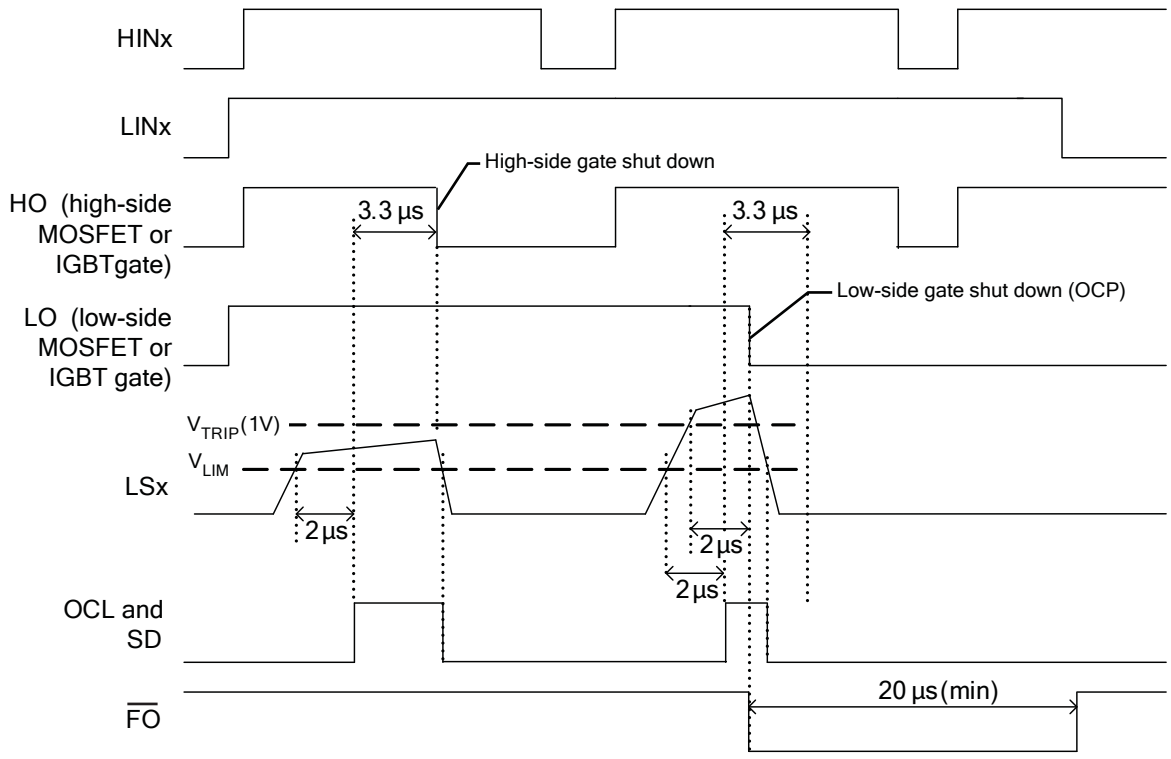


Figure 6. Timing Chart of Current Limiter Operation

the V_{UVHL} rated value, 10 V (typ), the high-side MOSFETs are shut down. When the voltage between VCC1 and COM1 goes below V_{UVLL}, 11 V (typ), which applies on both of VCC1 and VCC2 UVLO conditions, the high-side MOSFETs are shut down. After a shutdown, when the power supply voltage rises and exceeds V_{UVLH}, 11.5 V (typ), at the next positive (rising) edge (edge operation), an output-on pulse appears at HO.

Note: When power MOSFET output is shut down according to UVLO operation due to a voltage drop on the high side, the fault is not reflected at the $\overline{FO}$ output.

Figures 8 and 9 show the internal equivalent circuit of the UVLO detection features on the high-side control power supply, on the VB and VCC1 pins. As shown in the figures, internal filters are provided to eliminate line noise.

When the voltage between VCC2 and COM2 goes below V_{UVLL}, 11 V (typ), the low-side MOSFETs are shut down and the open collector internal transistor on the $\overline{FO}$ pin turns on. When VCC2 rises and exceeds V_{UVLH}, 11.5V(typ), the shut down of the low-side MOSFETs is released and internal transistor on the $\overline{FO}$ pin turns off. After the fault condition is released, the $\overline{FO}$ transistor operates according to LIN (logic level operation), see figure 10.

The low-side UVLO circuit has an internal filter to eliminate line noise, similar to the high-side UVLO circuit.

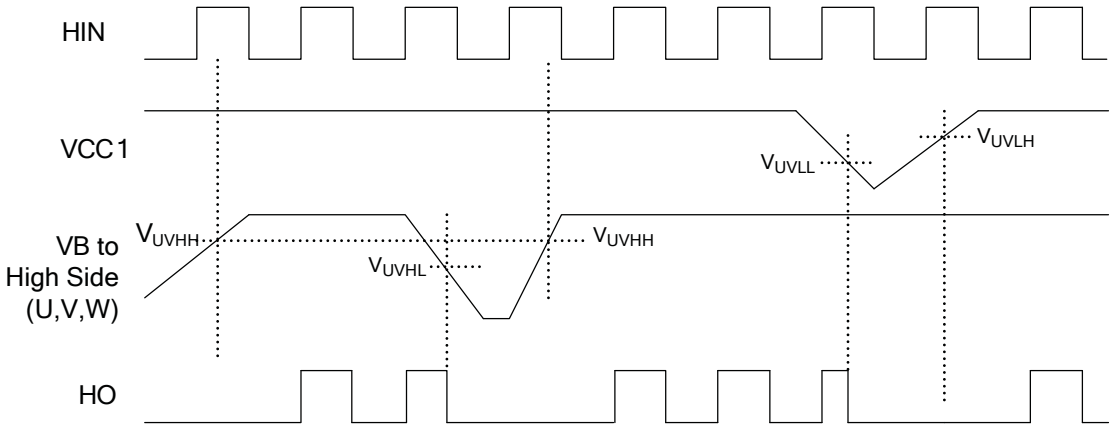


Figure 7. Timing Chart of High-Side UVLO Operation

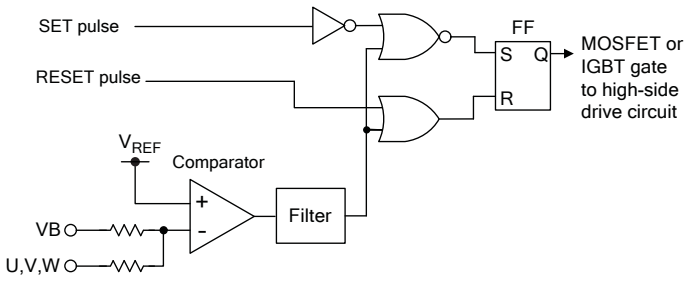


Figure 8. High-Side UVLO Internal Equivalent Circuit at VB

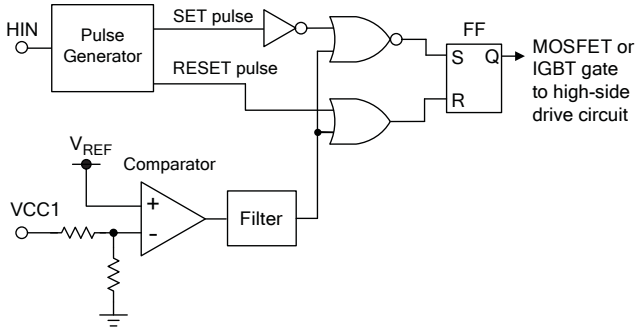


Figure 9. High-Side UVLO Internal Equivalent Circuit at VCC1

As mentioned above, this IC contains filters against steep drops in the control voltages: VB, VCC1, and VCC2. However, there are possibilities of malfunction due to line noise or IC damage in the event excessive voltage is applied, a filter time-constant is exceeded, or only VCC1 drops but VB is retained, and so forth. Therefore, please place an external ceramic capacitor, C_{BYP}, of 0.01 to 0.1 μF and a Zener diode, D_Z (V_Z = 18 to 20 V) near the power supply pins.

Thermal Shutdown (TSD)

The SIM6800M series contains a Thermal Shutdown circuit. In the event the IC is overheated by an increase of power consumption due to overload or an increase of ambient temperature, the low-side power MOSFETs are shut down, and the internal open collector transistor on the $\overline{FO}$ pin is turned on.

Table 4 provides the TSD temperature parameters. Detection is done by the low-side MIC. When the temperature exceeds 150°C (typ), the low-side MOSFETs are shut down, and when the temperature goes below 120°C (typ), the shutdown is released and the IC operates according to the LIN signals.

Note: Because the die temperature of the power MOSFETs is NOT directly monitored, damage to the IC by overheating cannot be fully prevented. Please note that there may be some delay in temperature detection, such as in cases when the MOSFET temperature is increased abruptly, until the heat reaches the monitors.

Table 4. Thermal Protection (TSD) Levels

		Low-Side MIC Temperature (°C)		
	Symbol	**Min.**	**Typ.**	**Max.**
TSD Enable	T_{DH}	135	150	165
TSD Release	T_{DL}	105	120	135
TSD Hysteresis	T_{DHYS}	–	30	–

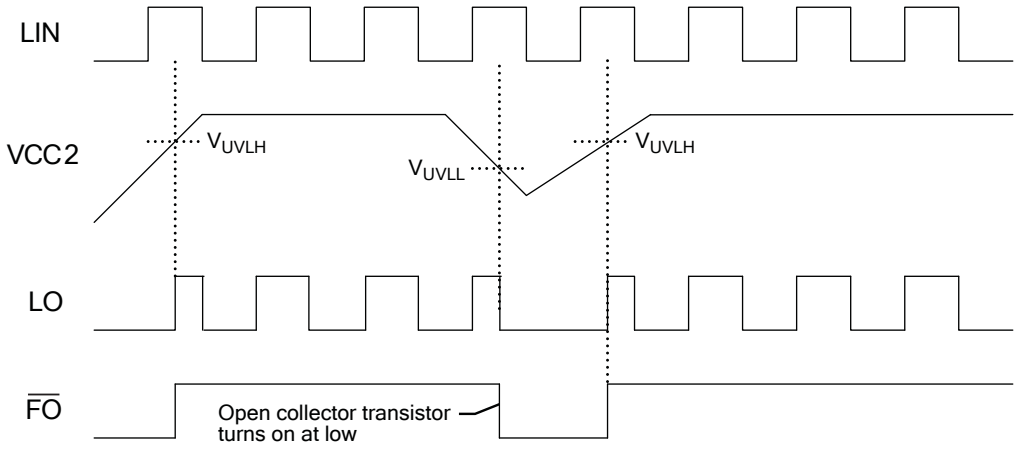


Figure 10. Timing chart of low-side UVLO operation

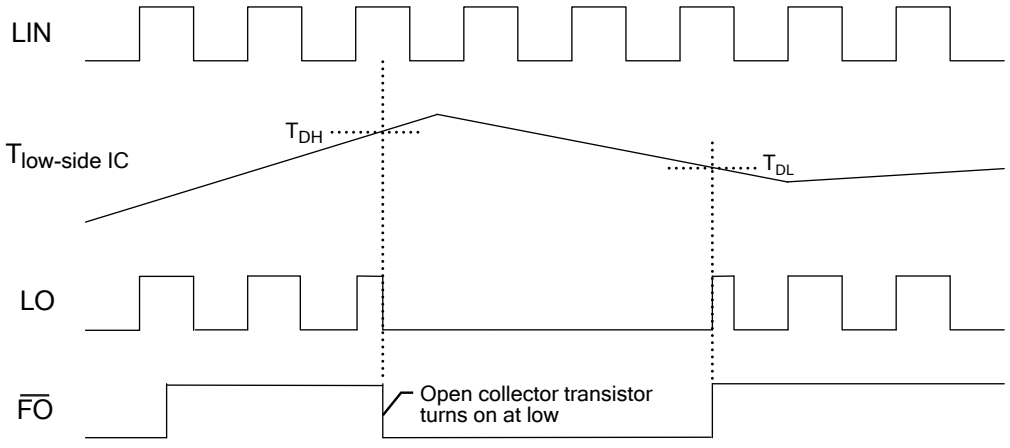


Figure 11. Timing Chart of Thermal Protection (TSD) Operation (T_{MIC} is the temperature monitored at the low-side MIC)

Over Current Protection (OCP)

The SIM6800M series contains an Overcurrent Protection function. Figure 12 shows the internal equivalent circuit structure for OCP. If the voltage between LSx and COM exceeds V_{TRIP}, 1.0 V (typ), for the blanking time, t_{BK}, 2 µs (typ), OCP operation is started.

At the start of OCP operation, at the same time as an internal transistor on the $\overline{FO}$ pin (connected to $\overline{FO}$ through a 50 Ω resistor) turns on, the gates of the low-side output MOSFETs are shut down. OCP operation is continued for a period of 25 µs (typ) after the OCP pin voltage becomes less than 1 V. After the 25 µs period has passed, the gate shutdown is released, and the transistor of the $\overline{FO}$ pin turns off. After that, the IC operates according to the LIN signals.

There is an internal circuit that shuts down the MOSFET gates when the $\overline{FO}$ pin is low. The $\overline{FO}$ Recovery time, the delay in return from OCP mode to normal operation, is adjustable by an external pull-up resistor, R_{FO}, on the $\overline{FO}$ pin. If it is required to extend the MOSFET shutdown period beyond the 25 µs (typ) of OCP, it can be extended by increasing the value of R_{FO} or not inserting R_{FO}. For more information, please refer to the Implementing Adjustable $\overline{FO}$ Recovery Time section.

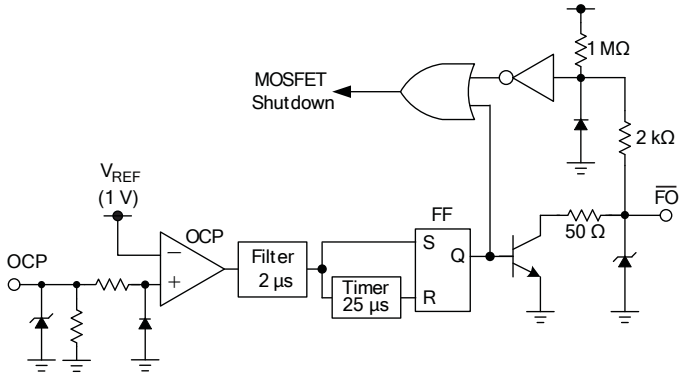


Figure 12. OCP Internal Equivalent Circuit

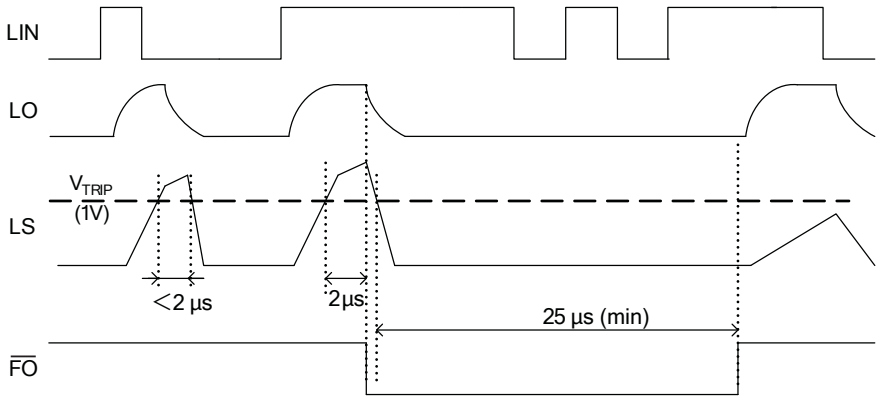


Figure 13. Timing Chart of Overcurrent Protection (OCP) Operation

Implementing Adjustable $\overline{FO}$ Recovery Time

This IPM has a function to adjust $\overline{FO}$ recovery time using an external pull-up resistor and a capacitor added at the $\overline{FO}$ pin. Figure 14 is an example for the implementation. Using this implementation the recovery time from an OCP mode to the normal operation can be increased. If the port of the MCU connected to $\overline{FO}$ has an internal pull-down resistor, the following calculation can be used:

$$V_{FO} \times R_{IN} / [(1\times10^6 \times R_{FO}) / (1\times10^6 + R_{FO}) + R_{IN}] \geq V_{th}$$

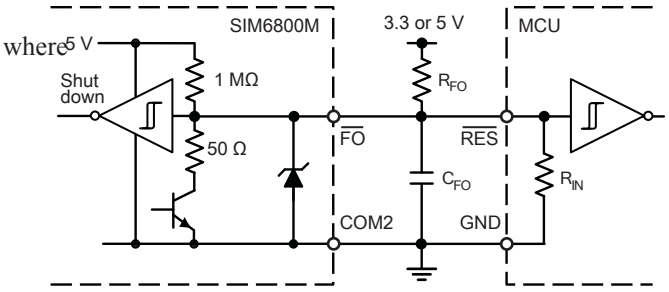


Figure 14. $\overline{FO}$ Internal Equivalent Circuit; demonstrating R_{FO} and C_{FO} implementation

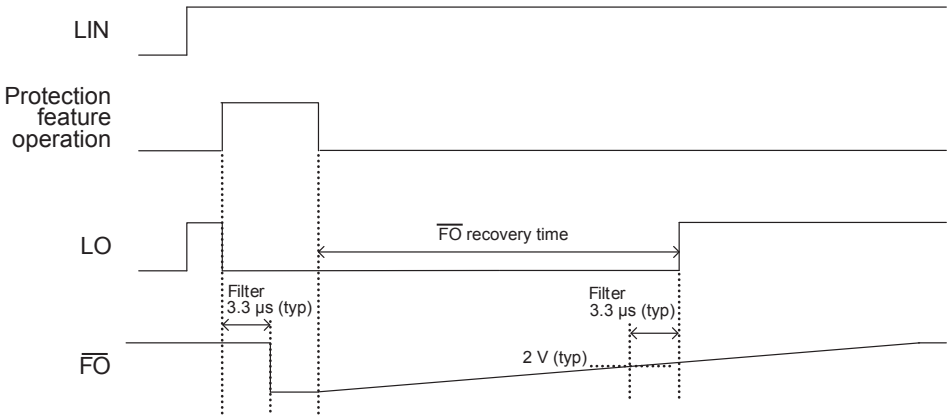


Figure 15. Timing Chart for $\overline{FO}$ Recovery

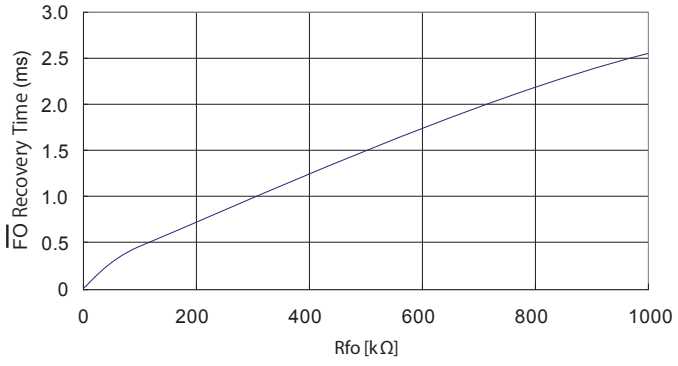


Figure 16. $\overline{FO}$ Recovery Time Versus R_{FO}; C_{FO} = 0.01 µF, V_{FO} = 5 V

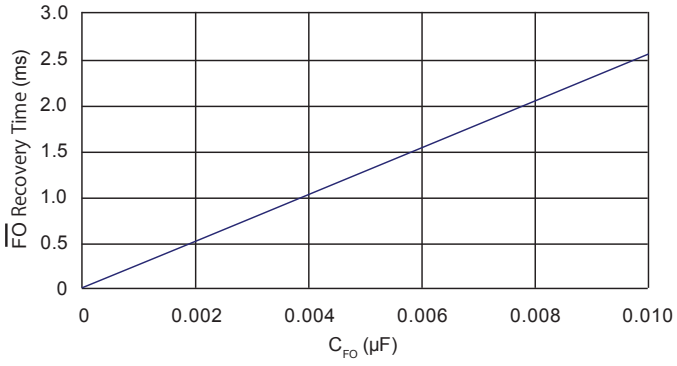


Figure 17. $\overline{FO}$ Recovery Time Versus C_{FO}; R_{FO} = 1 MΩ, V_{FO} = 5 V

Application Information

Figure 18 is an example of a typical application circuit.

- Please be sure to connect W1 and W2, and V1 and V2, on the printed circuit board.
- When the current limiter is not used, please leave the OCL pin open, and the SD pin open or connected to GND (when significant external noise is expected).
- Although the $\overline{FO}$ pin has an internal pull-up resistor of 1 MΩ, please connect a pull-up resistor R_{FO} between the $\overline{FO}$ pin and a 5 V or 3.3 V power supply in consideration a noise reduction capability. Please note, if the $\overline{FO}$ pin is connected to the 5 V or 3.3 V without the pull-up resistor, the thermal protection (TSD) function is disabled (low-side UVLO protection and Overcurrent Protection functions remain enabled).
- Place a ceramic capacitor, C_{FO} (0.001 to 0.01 μF) between the $\overline{FO}$ and COM2 pins to avoid malfunction due to noise.
- Make the PCB circuit layout between the bootstrap capacitors, C_{BOOTx} (≈ 1 μF) and the IC as short as possible to avoid malfunction due to noise.
- Place a ceramic capacitor, C_{BYP} (0.01 to 0.1 μF) between VCC1 and COM1, as well as VCC2 and COM2, to avoid malfunction due to noise. Make the PCB circuit layout between these capacitors and the IC as short as possible.
- Make the PCB circuit layout between current sense resistor, R_S, inserted between LSx and COM2, and the IC as wide and as short as possible to avoid malfunction due to noise.

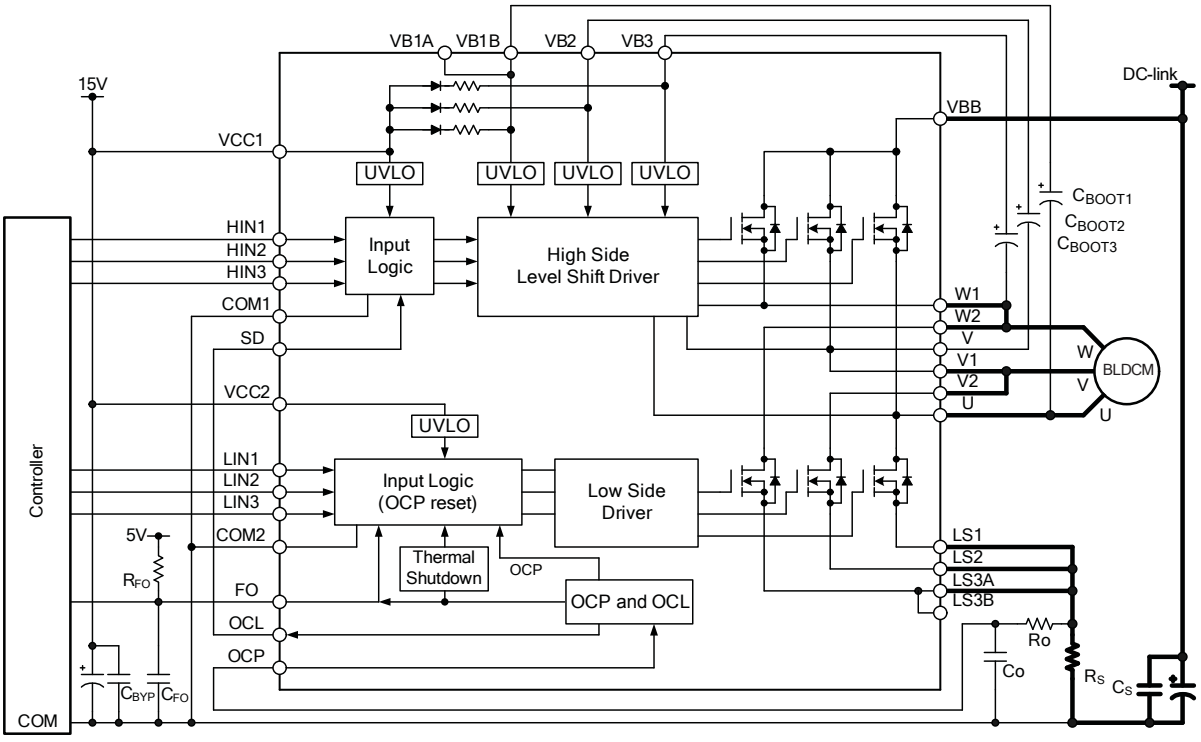


Figure 18. Typical Application Circuit; with a 5 V MCU (with current limiter configured)

Cautions and Warnings

• Power supply sequence

Powering-on the IC has no specific sequencing requirements. However, please ensure that the minimum controlling voltage, V_{CC}, has been established before sending input to the HIN or LIN pins.

• Short-circuit protection

This IC does not contain a protection circuit for ground-fault. Please make sure not to cause ground-fault mode.

• Distance between pins

The SIM6800M series uses a DIP 40-pin package and the distance between the pins is 1.778 mm pitch. It is recommended to apply overcoating or overmolding between the pins and on the PCB.

• Surge suppression

Please reduce applied surges to each pin by adding ceramic capacitors or Zener diodes, or other measures. Surges may cause not only malfunction but also damage the IC. Make sure to fully consider this point.

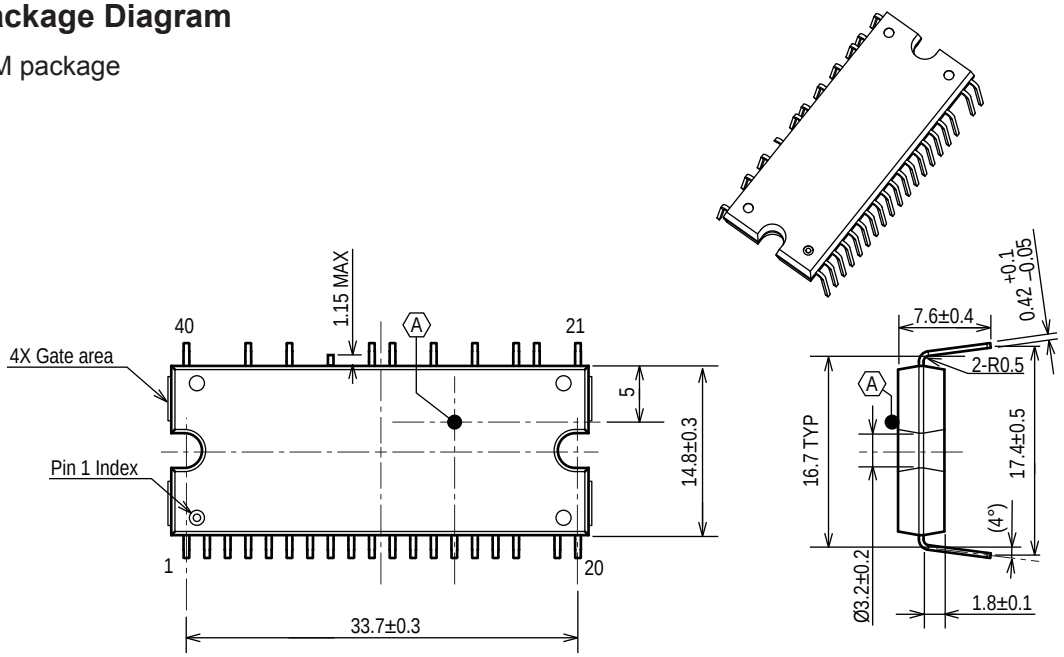
• Input dead-time

Please set dead-time externally (no internal setting), so as not to cause shoot-through (high to low short-circuit). 1.5 μs or longer is recommended for the SIM6800M series.

• To minimize interference between the current loop at the high voltage rail (VBB) and the +15 V power rail, the grounds for both power rails should be connected together on the PCB at a single point that is close to the frame ground or earth ground.

Package Diagram

SIM package



A Case temperature test point on branded surface, aligned with pin 14 at 5 mm from case side.

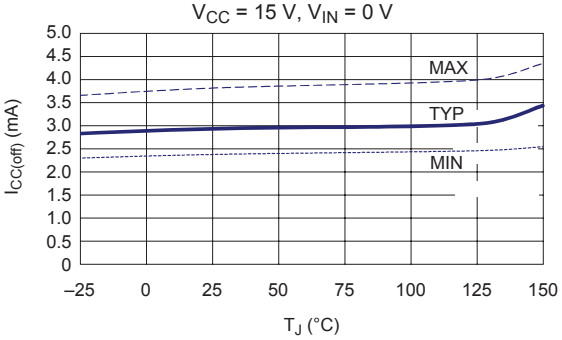
Pb-free. Device composition compliant with the RoHS directive.

Performance Characteristics

Applicable to all SIM6800 series

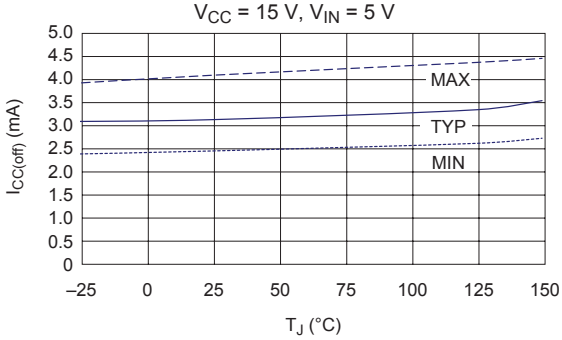
Supply Current (Off) versus Junction Temperature

V_{CC} = 15 V, V_{IN} = 0 V



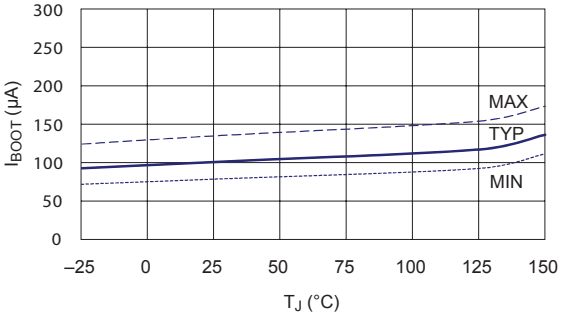
Supply Current (On) versus Junction Temperature

V_{CC} = 15 V, V_{IN} = 5 V



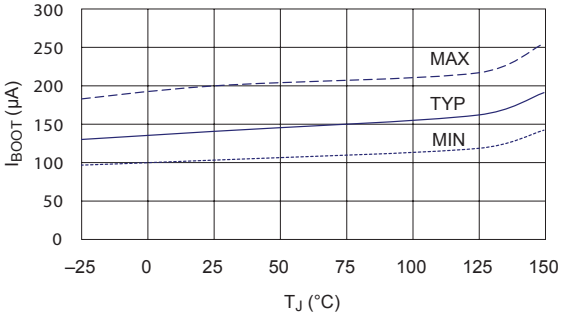
Boot Current (off) versus Junction Temperature

V_B = 15 V, one V_{HIN1} = 0 V



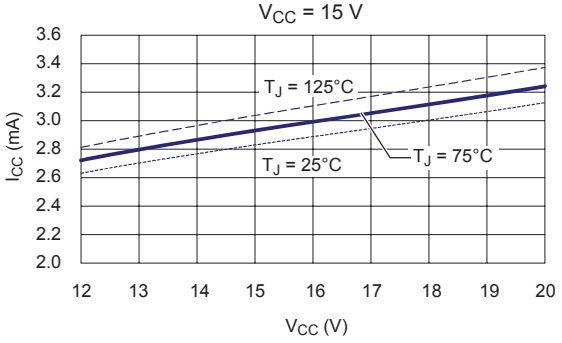
Boot Current (off) versus Junction Temperature

V_B = 15 V, V_{HIN1} = 0 V



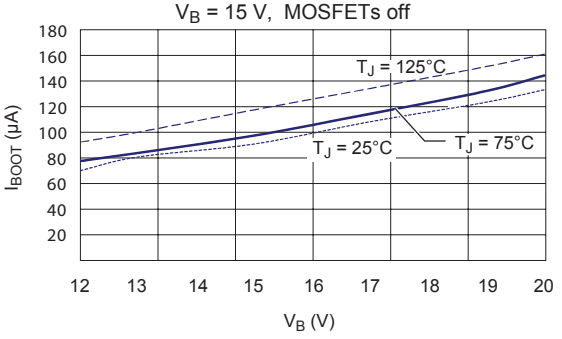
Supply Current versus Supply Voltage

V_{CC} = 15 V



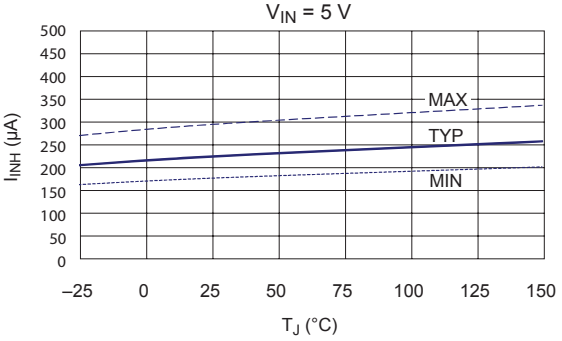
Boot Current (off) versus High Side Supply Voltage

V_B = 15 V, MOSFETs off



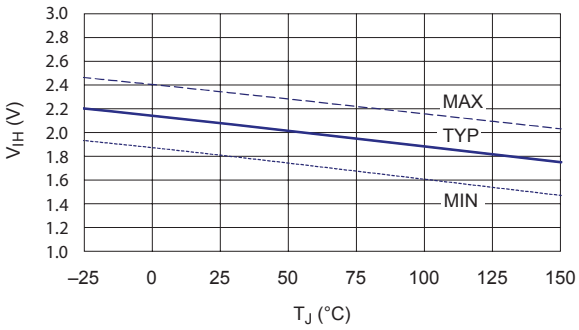
High-Side Input Current versus Junction Temperature

V_{IN} = 5 V

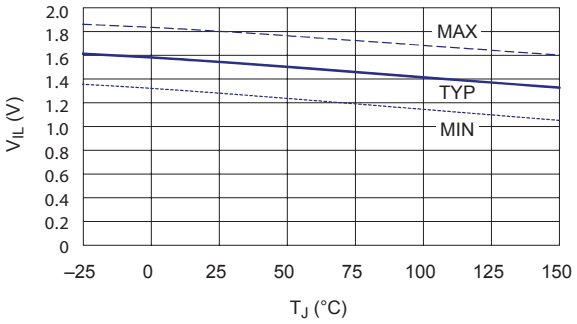


Applicable to all SIM6800 series

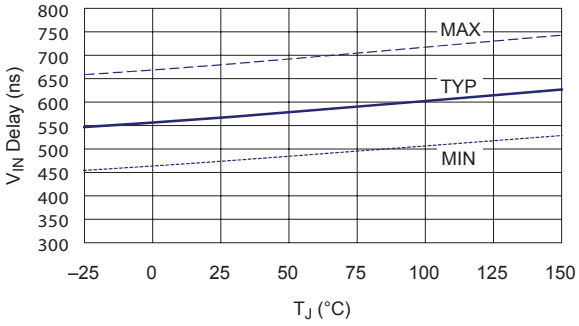
High-Side Input Voltage versus Junction Temperature



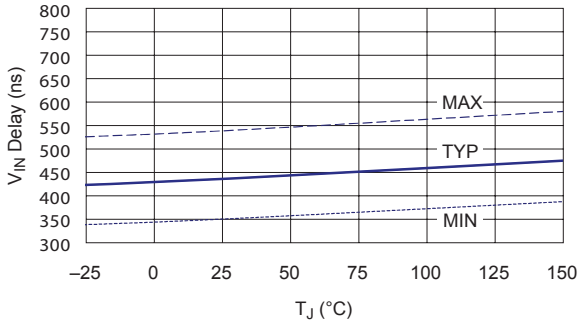
Low-Side Input Voltage versus Junction Temperature



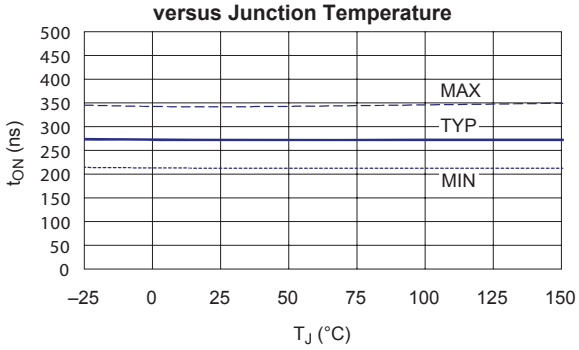
Input Delay versus Junction Temperature
V_{HIN} to V_{HO}



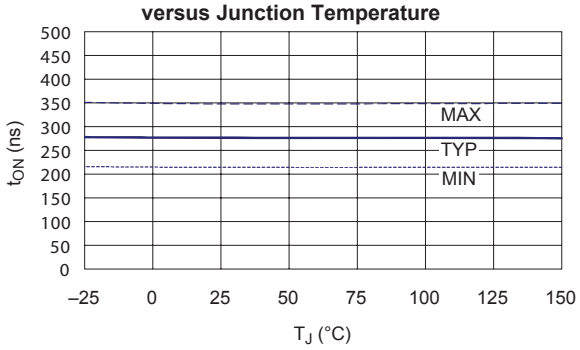
Input Delay versus Junction Temperature
V_{LIN} to V_{LO}



Minimum On-Time (High-Side) versus Junction Temperature

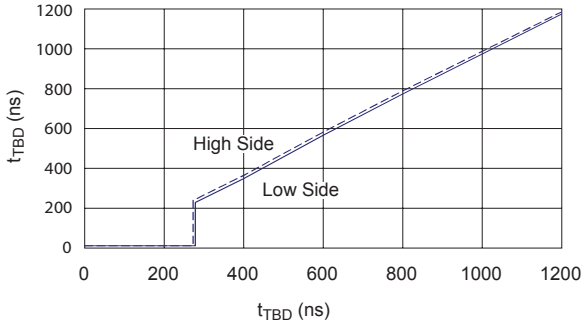


Minimum On-Time (Low-Side) versus Junction Temperature

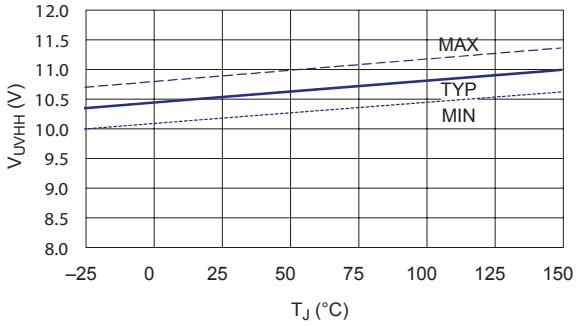


Output Gate Pulse Width versus Input Pulse Width

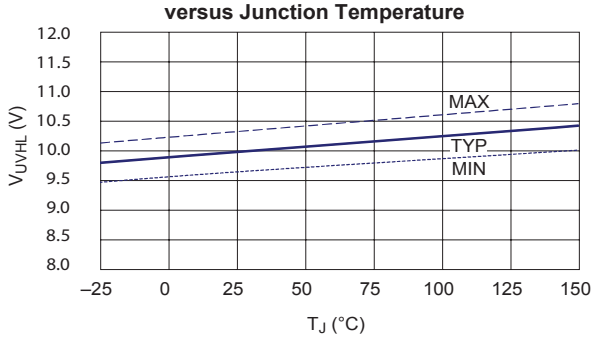
Typical, T_J = 25°C, V_{CC} = 15 V



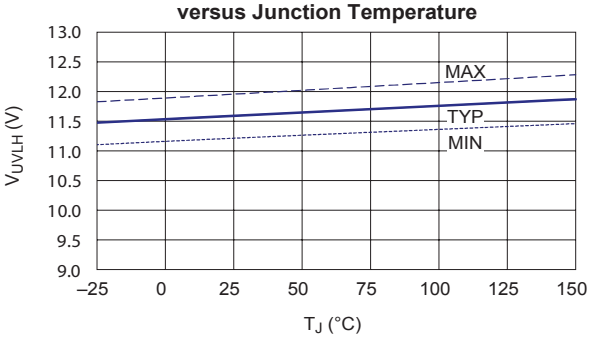
High-Side UVLO Release Threshold versus Junction Temperature



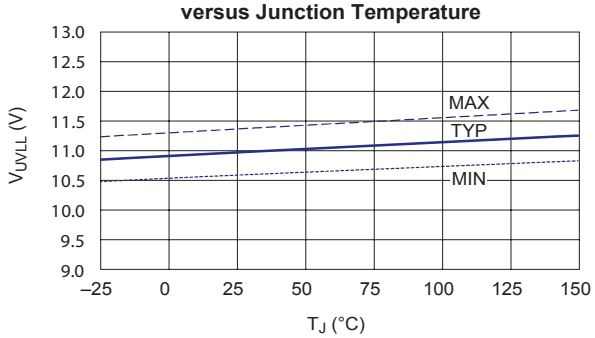
High-Side UVLO Enable Threshold versus Junction Temperature



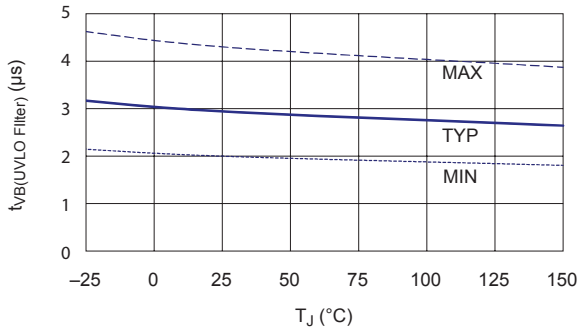
Low-Side UVLO Release Threshold versus Junction Temperature



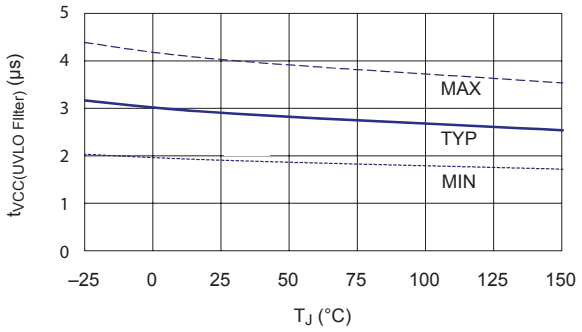
Low-Side UVLO Enable Threshold versus Junction Temperature



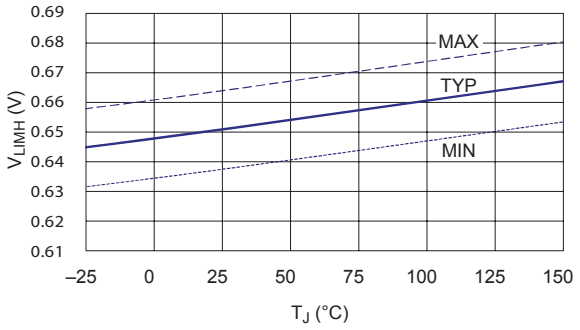
High-Side UVLO Filter Delay versus Junction Temperature



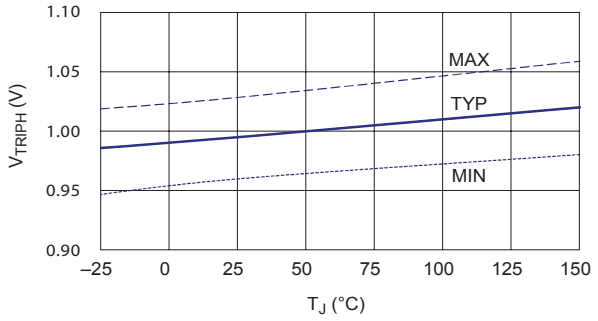
Low-Side UVLO Filter Delay versus Junction Temperature



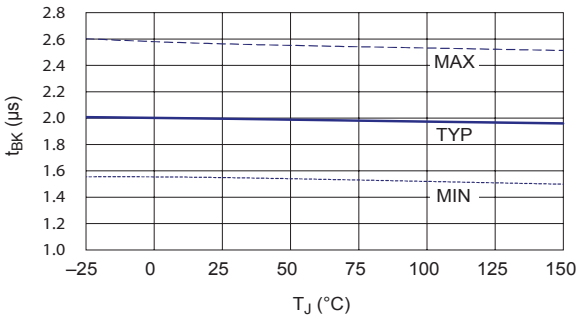
Overcurrent Limit (High) versus Junction Temperature



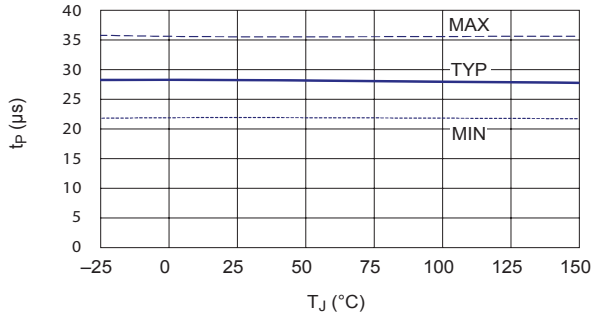
Overcurrent Trip Voltage (High) versus Junction Temperature



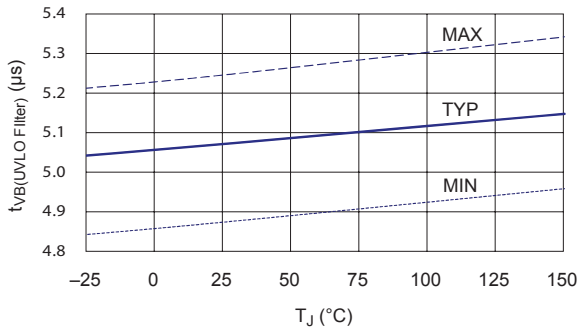
Overcurrent Blanking TIme versus Junction Temperature



OCP Hold-Time versus Junction Temperature

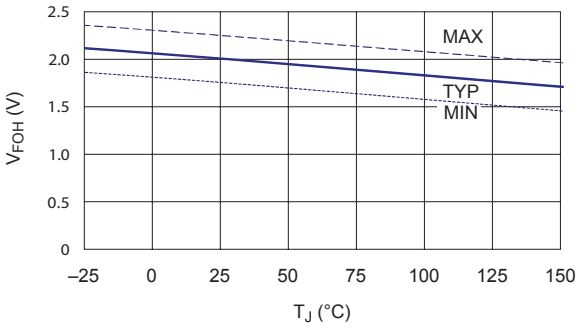


OCL Pin Output Voltage versus Junction Temperature

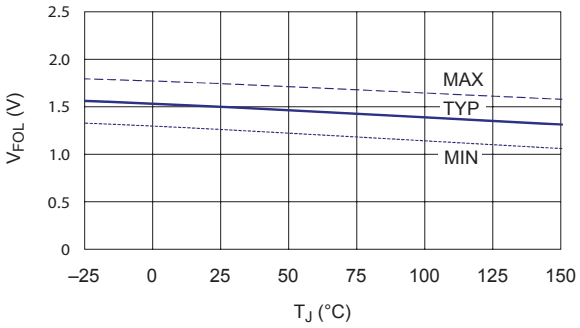


Applicable to all SIM6800 series

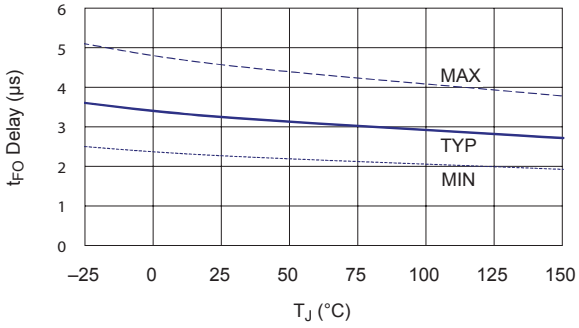
FO Input Voltage (On) versus Junction Temperature



FO Intput Voltage (Off) versus Junction Temperature

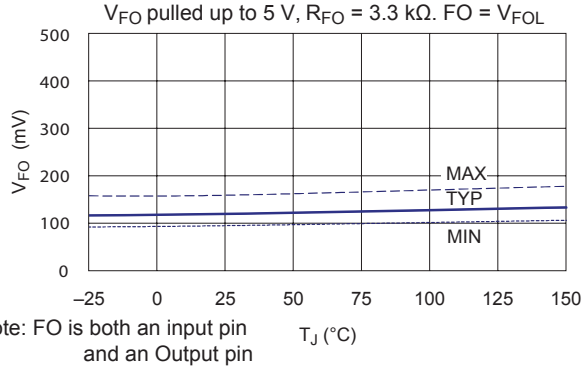


FO Input Filter Delay versus Junction Temperature



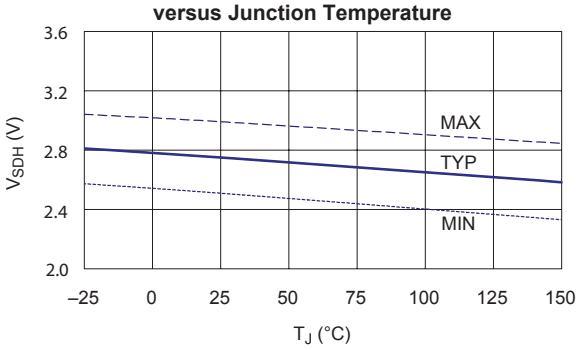
FO Output* Voltage versus Junction Temperature

V_{FO} pulled up to 5 V, R_{FO} = 3.3 kΩ. FO = V_{FOL}

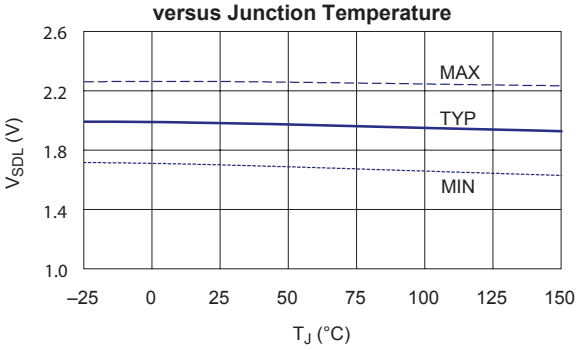


Note: FO is both an input pin and an Output pin

SD Input Voltage (On) versus Junction Temperature

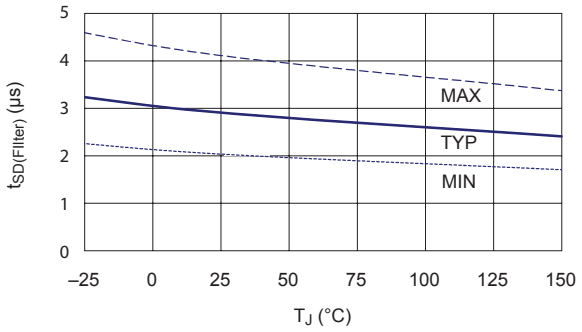


SD Input Voltage (Off) versus Junction Temperature



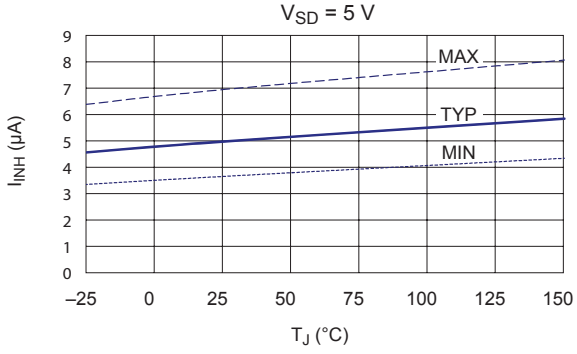
Applicable to all SIM6800 series

SD Input Filter Delay versus Junction Temperature



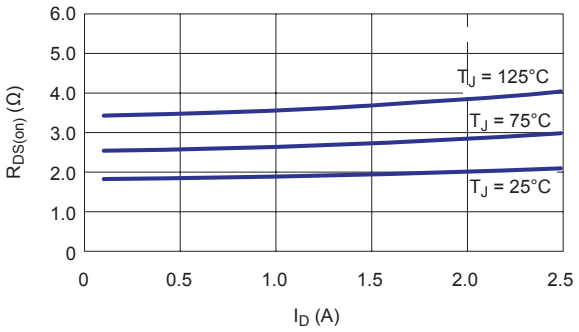
SD Input Current versus Junction Temperature

V_{SD} = 5 V

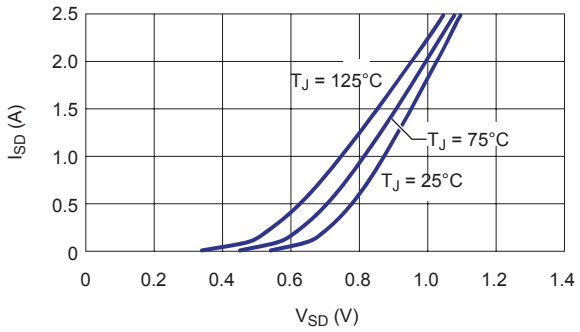


SIM6812M MOSFET Characteristics

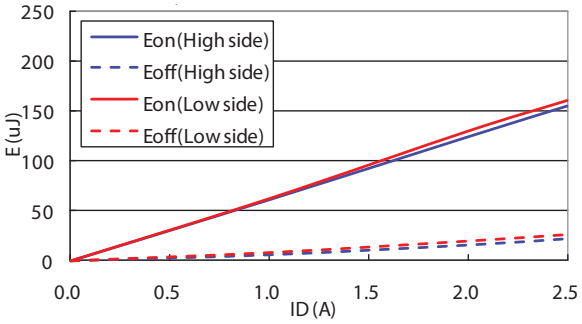
MOSFET On-Resistance versus Drain Current
V_{GS} = 15 V



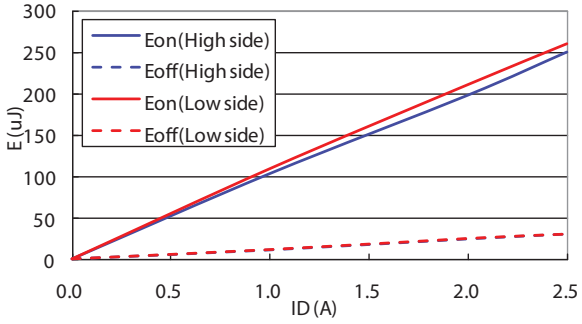
MOSFET On-Resistance versus Drain Current
V_{GS} = 0 V



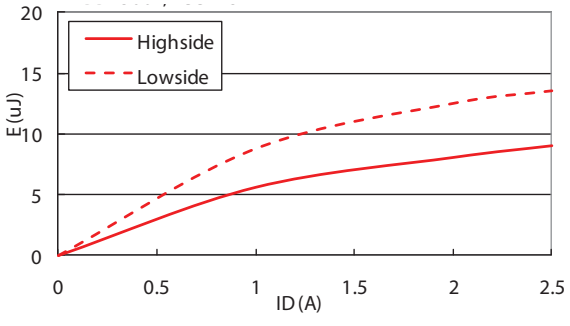
Switching Loss versus Drain Current
T_C = 25°C, V_{BB} = 300 V, V_{CC} = 15 V



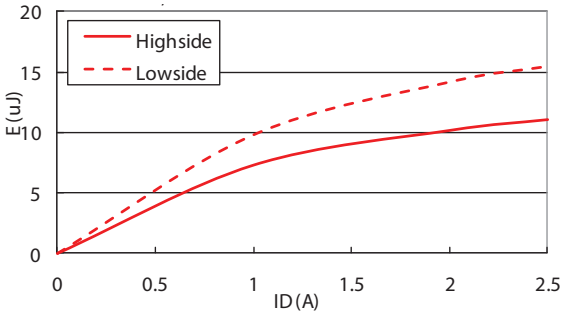
Switching Loss versus Drain Current
T_C = 125°C, V_{BB} = 300 V, V_{CC} = 15 V



Recovery Loss versus Drain Current
T_C = 25°C, V_{BB} = 300 V, V_{CC} = 15 V

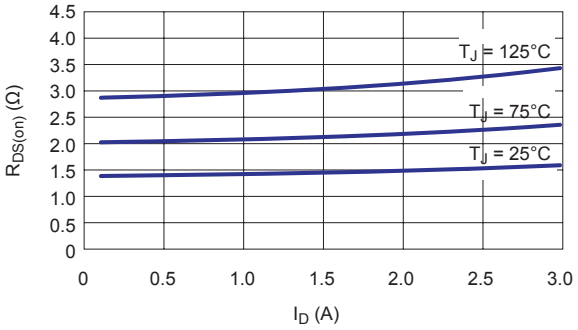


Recovery Loss versus Drain Current
T_C = 125°C, V_{BB} = 300 V, V_{CC} = 15 V

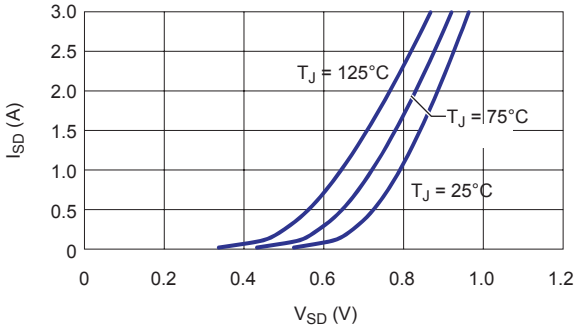


SIM6813M MOSFET Characteristics

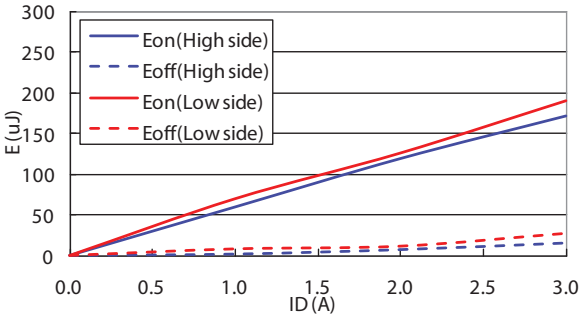
MOSFET On-Resistance versus Drain Current
V_{GS} = 15 V



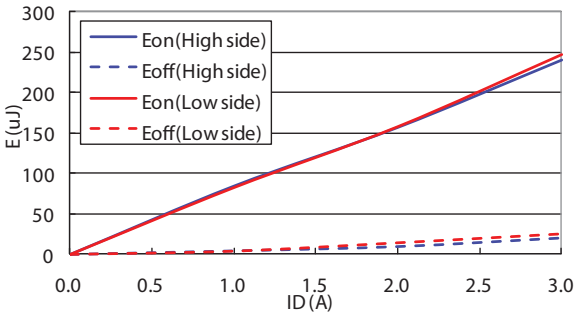
MOSFET On-Resistance versus Drain Current
V_{GS} = 0 V



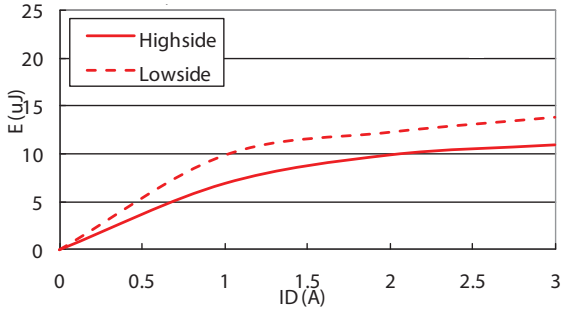
Switching Loss versus Drain Current
T_C = 25°C, V_{BB} = 300 V, V_{CC} = 15 V



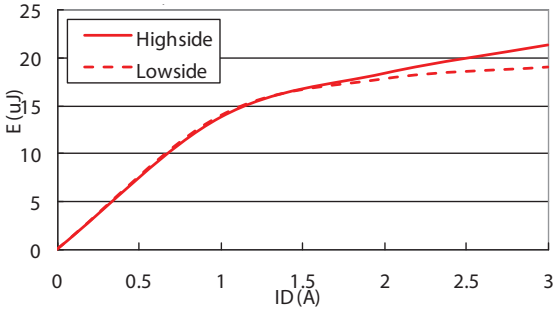
Switching Loss versus Drain Current
T_C = 125°C, V_{BB} = 300 V, V_{CC} = 15 V



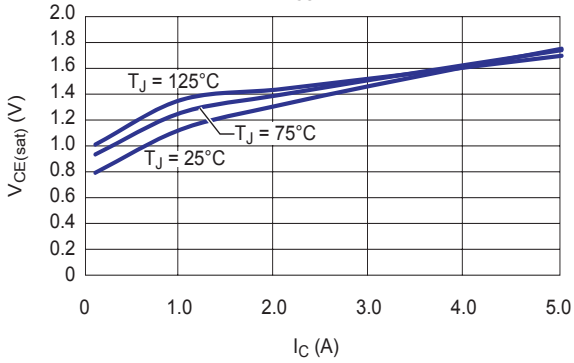
Recovery Loss versus Drain Current
T_C = 25°C, V_{BB} = 300 V, V_{CC} = 15 V



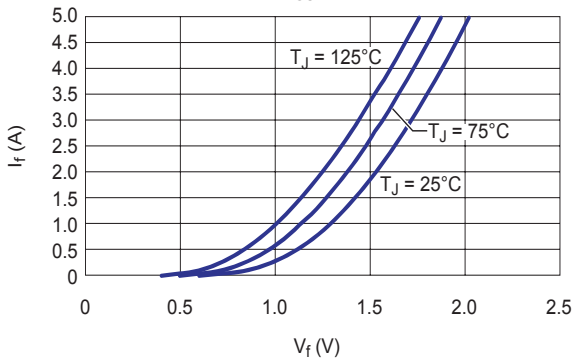
Recovery Loss versus Drain Current
T_C = 125°C, V_{BB} = 300 V, V_{CC} = 15 V



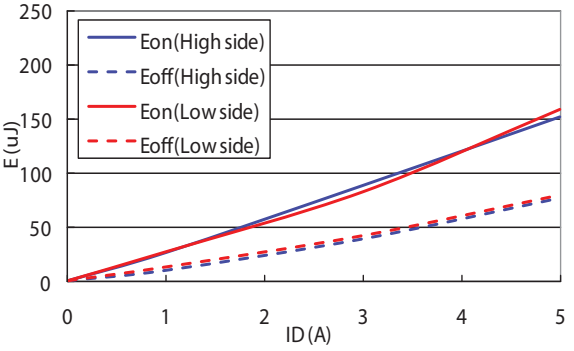
MOSFET On-Resistance versus Drain Current
V_{GS} = 15 V



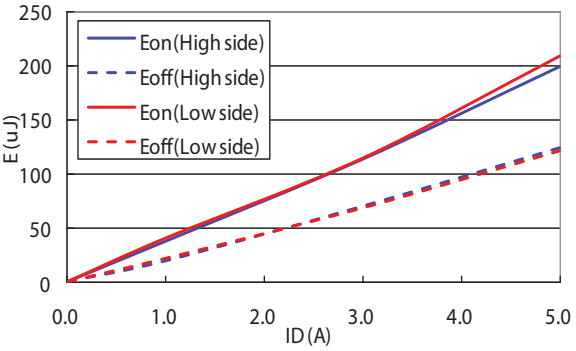
MOSFET On-Resistance versus Drain Current
V_{GS} = 0 V



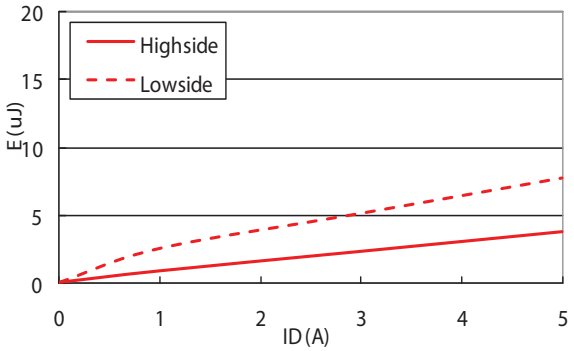
Switching Loss versus Drain Current
T_C = 25°C, V_{BB} = 300 V, V_{CC} = 15 V



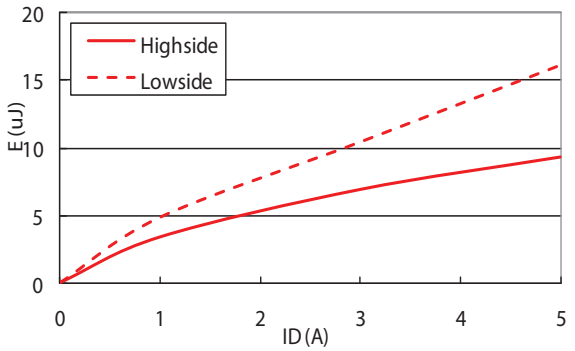
Switching Loss versus Drain Current
T_C = 125°C, V_{BB} = 300 V, V_{CC} = 15 V



Recovery Loss versus Drain Current
T_C = 25°C, V_{BB} = 300 V, V_{CC} = 15 V

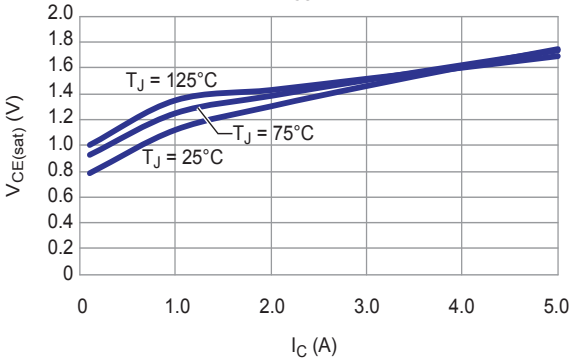


Recovery Loss versus Drain Current
T_C = 125°C, V_{BB} = 300 V, V_{CC} = 15 V

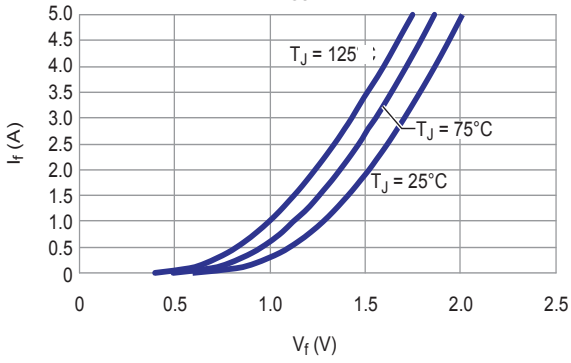


SIM6827M IGBT Characteristics

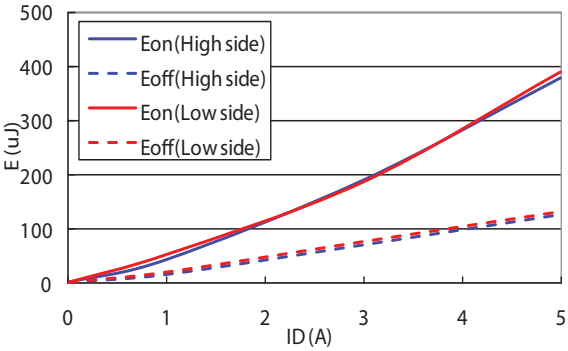
MOSFET On-Resistance versus Drain Current
V_{GS} = 15 V



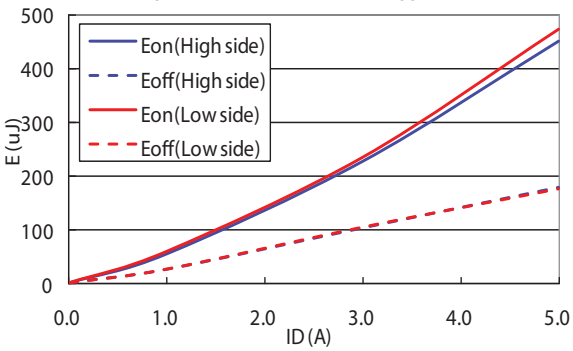
MOSFET On-Resistance versus Drain Current
V_{GS} = 0 V



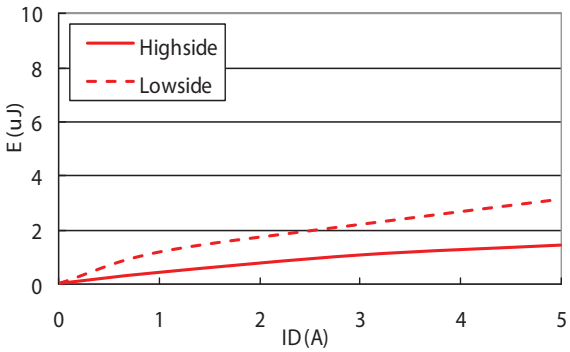
Switching Loss versus Drain Current
T_C = 25°C, V_{BB} = 300 V, V_{CC} = 15 V



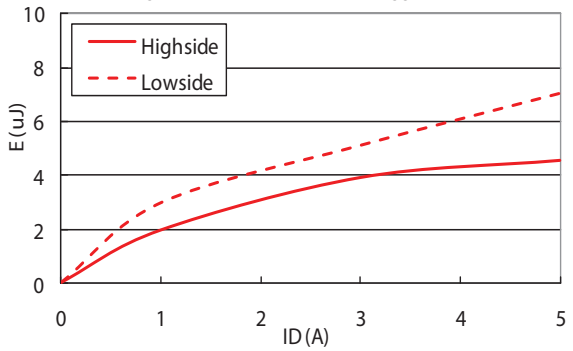
Switching Loss versus Drain Current
T_C = 125°C, V_{BB} = 300 V, V_{CC} = 15 V



Recovery Loss versus Drain Current
T_C = 25°C, V_{BB} = 300 V, V_{CC} = 15 V



Recovery Loss versus Drain Current
T_C = 125°C, V_{BB} = 300 V, V_{CC} = 15 V



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