CMOS timing base timer

product presentation

ICM 7555 is the CMOS version of the 5 55 series universal timer. This device provides precise time delay and frequency with low power loss and power supply current spikes. When the chip is used as a trigger delay, the time delay is precisely controlled by a single external resistor and capacitor. In stable mode, the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor.

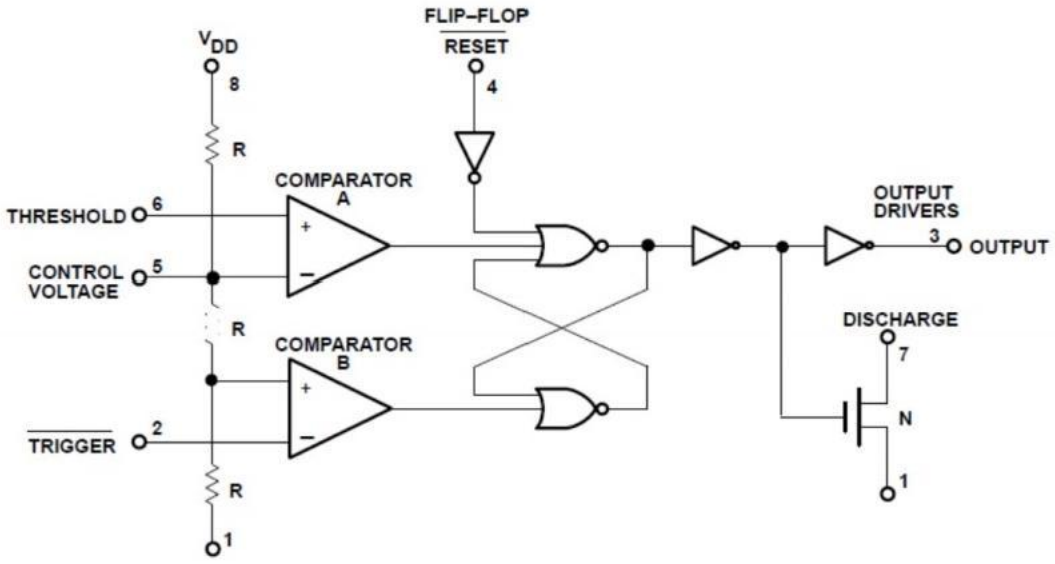
main features

- Low power supply current: 80 uA (typical value)
- Steady state frequency capability of 500 KHz.
- Minimum operating voltage 4.5V.
- At 5V voltage, the output is completely compatible with TTL and CMOS logic voltage.
- The power supply current spike is low during the output conversion.
- Very low trigger, threshold and reset current: 20pA (typical value).
- Operates in non-stable and monostable modes, with adjustable duty cycle.
- Compatible with 555 series timer pins.
- DIP/SOP8 package is adopted.

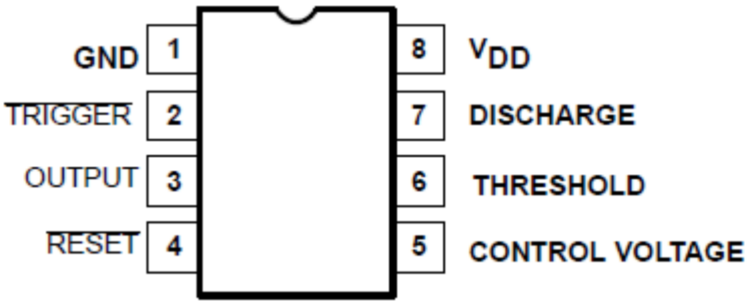
Product application

- pulser
- Precise timing
- Delayed generation
- Pulse width modulation

Internal block diagram


FLIP–FLOP
RESET
4
VDD
8
R
COMPARATOR
A
THRESHOLD
6
CONTROL
VOLTAGE
5
R
COMPARATOR
B
TRIGGER
2
R
1
OUTPUT
DRIVERS
3
OUTPUT
DISCHARGE
7
N
1

Pin description



truth table

RESET	Vtrigger	Vthreshold	OUTPUT	DISCHARGE SWITCH
LOW	--	--	LOW	ON
HIGH	<1/3VCC	--	HIGH	OFF
HIGH	>1/3VCC	>2/3VCC	LOW	ON
HIGH	>1/3VCC	<2/3VCC	as what mentioned before	

Limit parameters (note 2)

symbol	parameter	price	unit
Vcc	service voltage	15	V
Toper	operating temperature range	-20~85	℃
Tj	junction temperature	150	℃
Tstg	Storage temperature range	-50~150	℃

Recommended working conditions (TA=25℃)

symbol	parameter	price	unit
Vcc	service voltage	0~15	V
Vth, Vtrig, VCTRL, Vreset	maximum input voltage	-0.3~Vcc+0.3	V

Electrical characteristics (note 1,2)

Conditions:(no special provisions, in the test circuit, TA = 25℃, all switches are open, RESET is connected to VCC)

parameter	characteristic	test condition	Min	representative value	Max	unit
source current	Is	VCC=5V		30	50	uA
		VCC=10V		60	100	
		VCC=15V		90	150	
control voltage	VCTRL	VCC=5V	3.28	3.33	3.38	V
		VCC=10V	6.6	6.66	6.7	

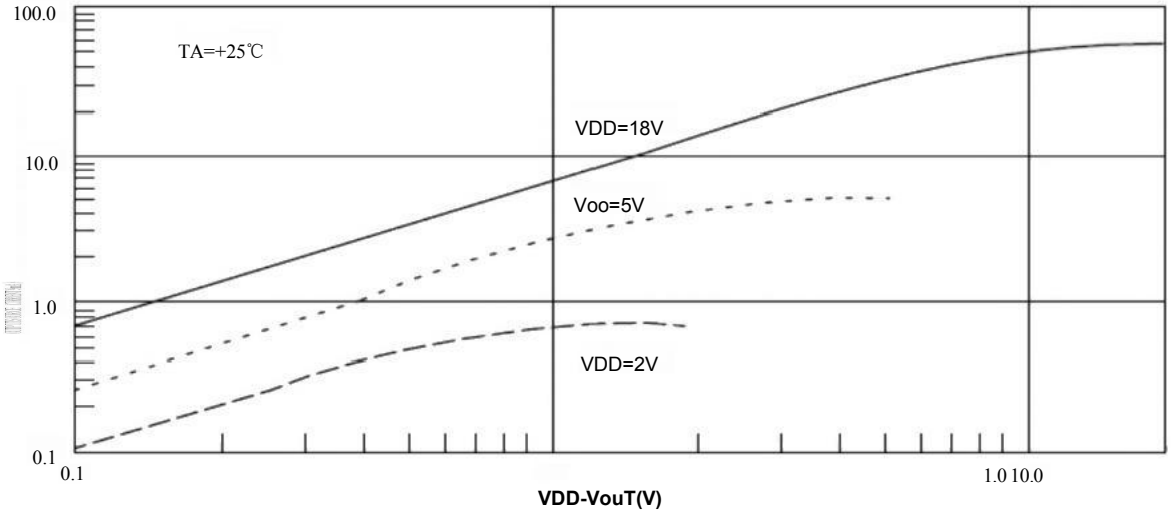
		VCC=15V	9.95	10	10.15	
parameter	characteristic	test condition	Min	representative value	Max	unit
Discharge terminal saturation voltage	VDIS	VCC=5V, IDIS=10mA		100	400	mV
Output voltage (low)	VOL	VCC=5V, Io=3.2mA		0.1	0.4	V
		VCC=15V, Io=3.2mA				
Output voltage (high)	VOH	VCC=5V, Io=-2mA	4.0	4.5		V
		VCC=15V, Io=-2mA	14.5	14.75		
trigger voltage	VTRIG	VCC=5V	1.55	1.66	1.7	V
		VCC=10V	3.23	3.33	3.38	
		VCC=15V	4.95	5	5.05	
Trigger current	ITRIG	VCC=5V		10		pA
Reset voltage	VRES	VCC=5V	0.4	0.7	1.2	V
Reset current	IRES	VCC=5V		10		pA
threshold current	ITHRESH	VCC=5V		10		pA
Discharge terminal leakage current	IDIS	VCC=12V		1.0	100	nA
Output goes up	tR	VCC=5V, RL=10MQ, CL=10pF	35	40	75	ns
drop-out time	tF	VCC=5V, RL=10MQ, CL=10pF	35	40	75	ns
maximun-frequency	Fmax			500		KHz

Note 1: All voltages are measured relative to the ground pin unless otherwise specified.

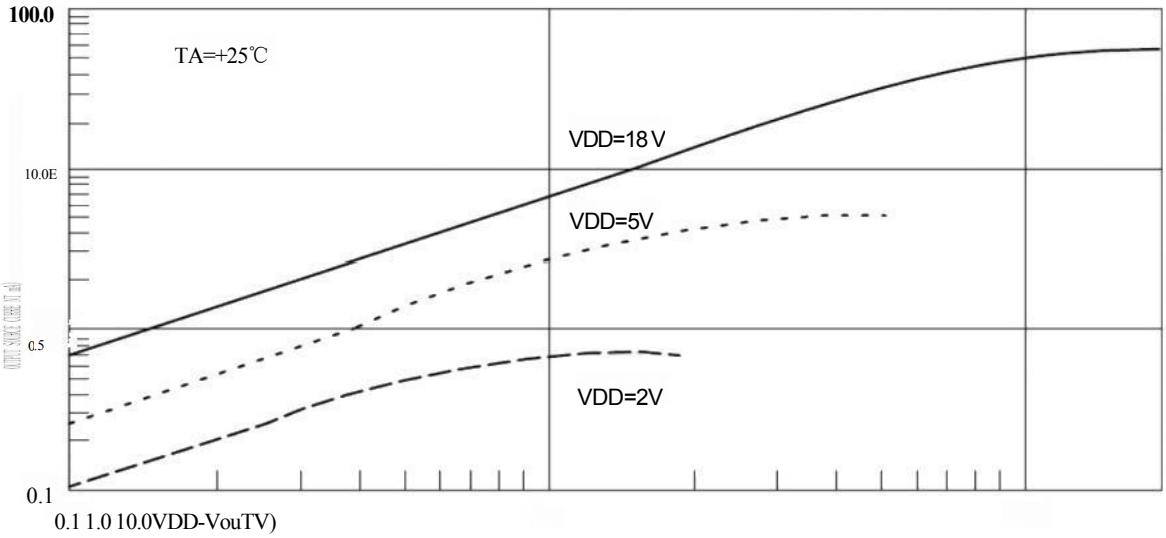
Note 2: The absolute maximum rating indicates that exceeding this operating limit may result in chip damage. The operating rating indicates that the device can function but does not guarantee specific performance limits. Electrical characteristic test conditions ensure DC and AC electrical specifications under certain performance indicators. This assumes that the chip is within its operating range. Specifications do not guarantee parameters without restrictions; however, typical values are a good indication of chip performance.

Typical performance

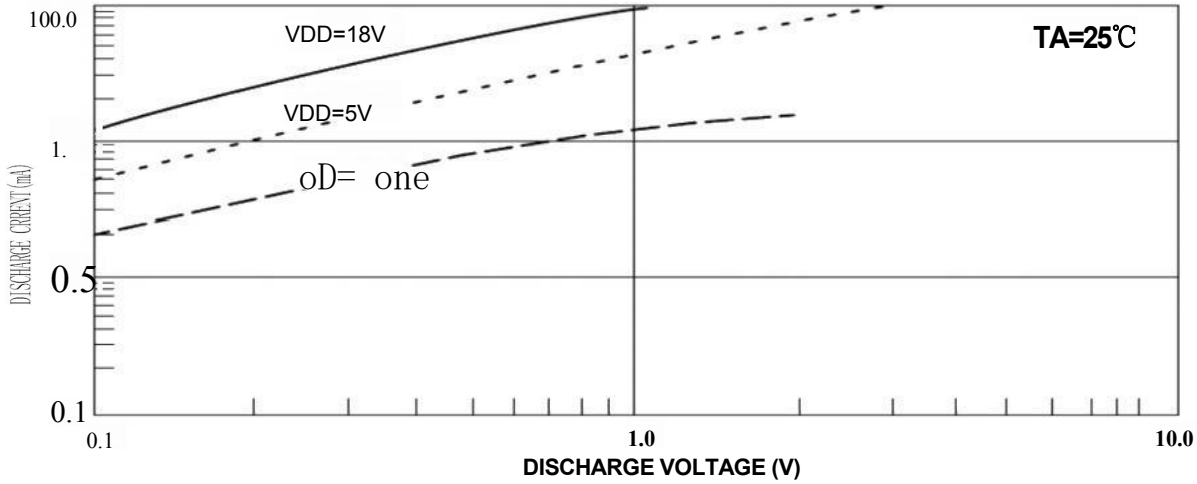
1. High output voltage drop and output source current



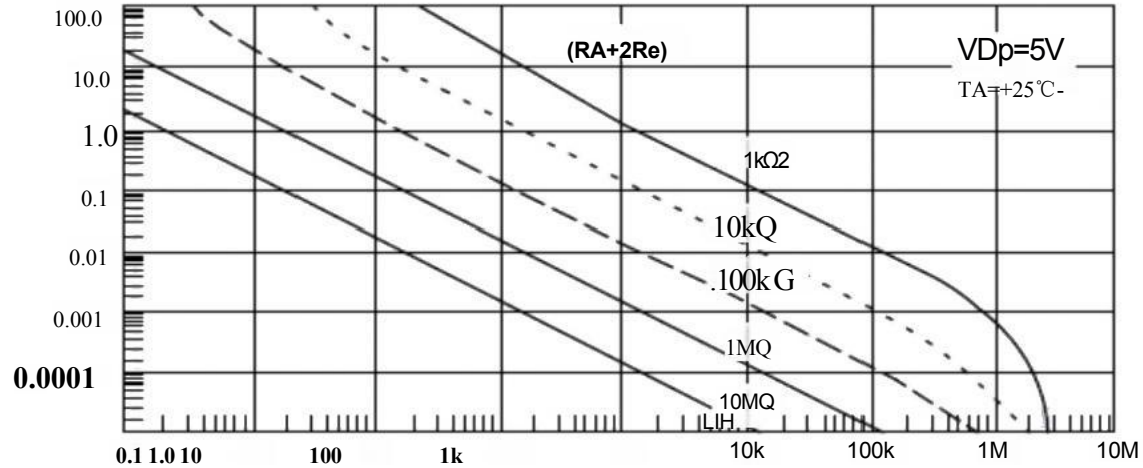
2. Low output voltage and output absorption current



3. Low discharge output voltage and discharge absorption current



4. Ra, Rb, C and frequency

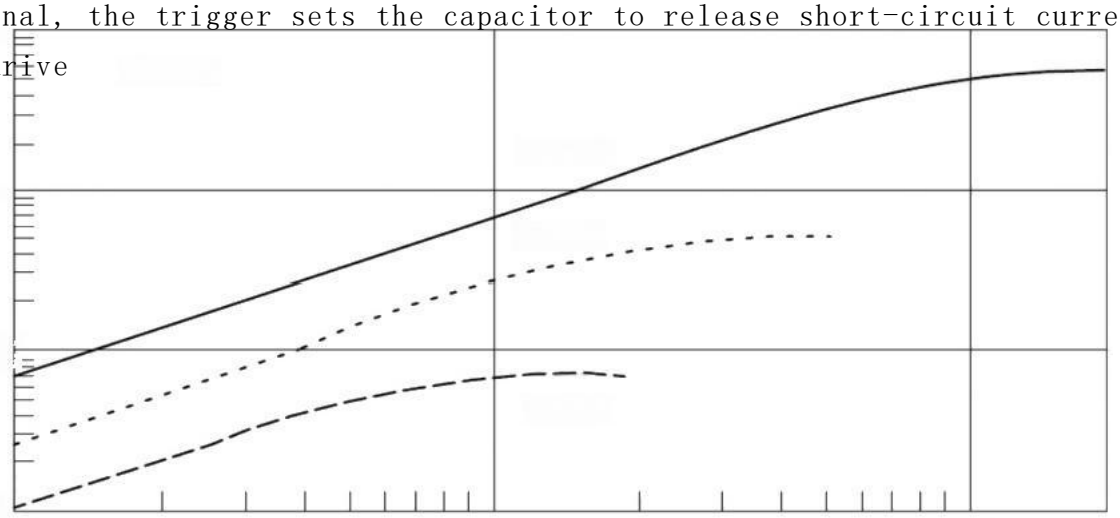


application message

monostability

In this mode of operation, the timer acts as a trigger (Figure 1). The external capacitor is initially discharged through the internal circuit. When a negative trigger pulse less than 1/3 VS is applied to the trigger

terminal, the trigger sets the capacitor to release short-circuit current and drive



The output is high.

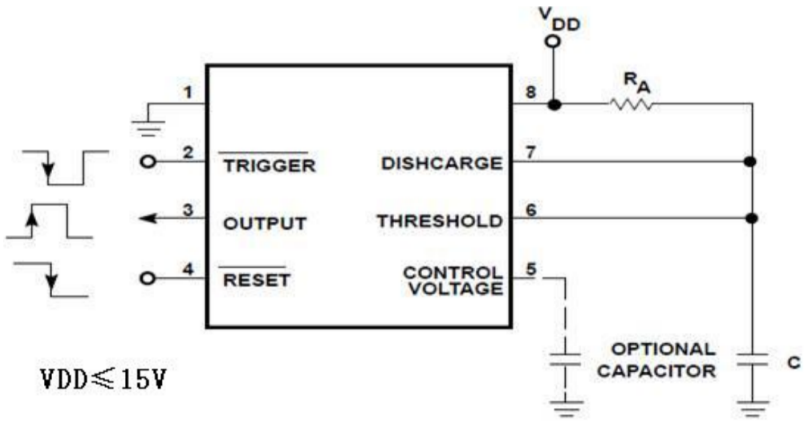


Figure 1: Monostable (single)

steady-state operation

The circuit is connected as shown in Figure 2 (the trigger and the threshold terminals are connected together), which triggers itself and releases the operation as a multivibrator. The external capacitor is charged through RA+ RB and discharged through RB. Thus, the duty cycle can be precisely set by the ratio of these two resistors.

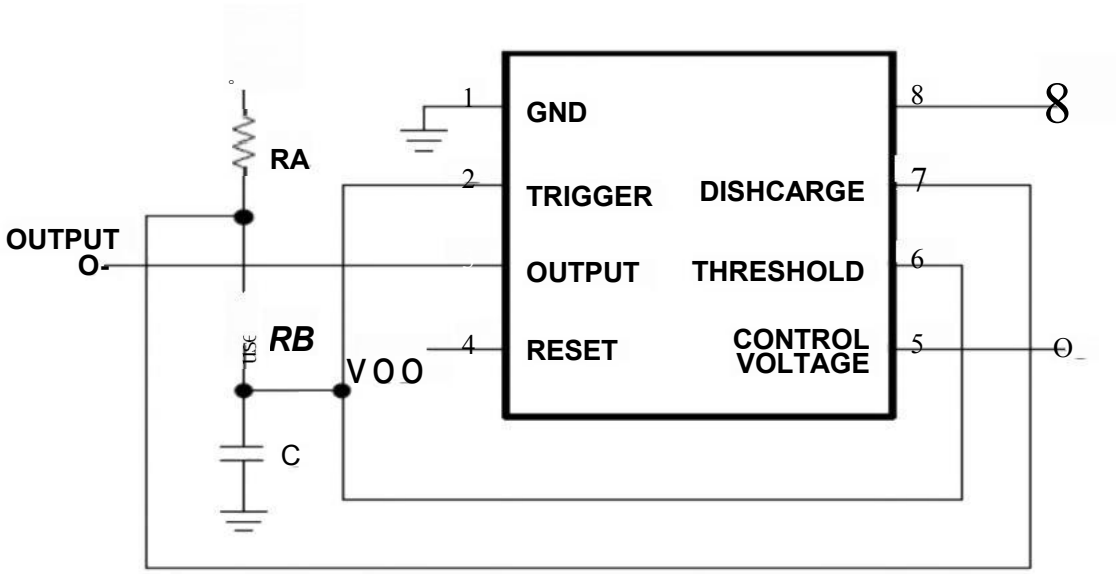
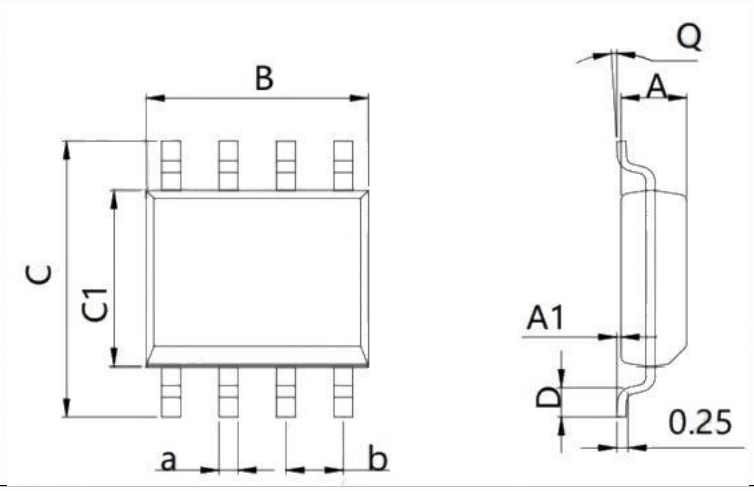


Figure 2: Steady state (variable duty cycle oscillator)

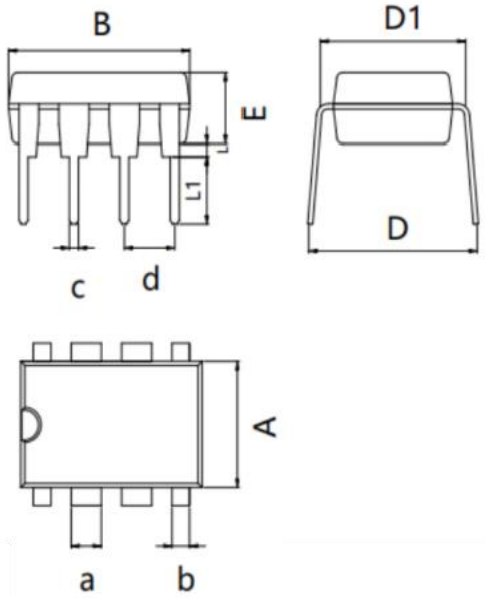
Package dimensions

SOP8



Dimensions In Millimeters(SOP8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

DIP8



DimensionsIn Millimeters(DIP8)											
Symbol:	A	B	D	D1	E	L	L1	a	b	C	d
Min:	6.10	9.00	8.40	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	9.00	7.82	3.55	0.70	3.60	1.55	0.90	0.50	